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A Novel Plus Type DVCC-Based Current-Mode Biquad

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Abstract: This paper presents a novel current-mode biquad using only plus type DVCCs (differential voltage current conveyors). The circuit enables LP (low-pass), BP (band-pass), HP (high-pass), BS (band-stop) and AP (all-pass) responses by the selection and/or addition of the circuit currents with no component matching constraints. Moreover the circuit parameters ω_0 and Q can be set orthogonally adjusting the circuit components. An achievement example is given together with simulation results by PSPICE.

Key words: Analog circuits, biquad responses, plus type DVCCs.

1. Introduction

High performance active circuits have received much attention. The circuit designs using active devices such as CCIIs (second generation current conveyors), the DVCCs (differential voltage current conveyors) and so on have been reported in Refs. [1-4].

A DVCC is a very useful active device, and DVCC-based circuit is adaptable to wide band operation. A plus type DVCC is composed of simpler circuit configuration than a minus type one. Hence it has wide band operation and low power performance compared with the minus type DVCC.

Till now several biquads employing the DVCCs have been discussed [2-4]. However, plus type DVCC-based biquad [4] has not yet been studied sufficiently.

This paper introduces a novel current-mode biquad. First we show a basic current-mode biquad using only the plus type DVCCs and grounded passive components. Then typical current-mode biquad is consisted of using the basic current-mode one. The circuit enables LP (low-pass), BP (band-pass), HP (high-pass), BS (band-stop) and AP (all-pass) responses by the selection and/or addition of the input and output currents with no component matching constraints. And the circuit parameters ω_0 and Q can be set orthogonally by the circuit components.

The achievement example is given with PSPICE simulations, and the circuit workability is confirmed.

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2. DVCC and Its Performance

The symbol of the plus type DVCC is given in Fig. 1, and Fig. 2 shows the DVCC with MOS transistors. The plus type DVCC is characterized by the following terminal equation:

$$V_x = V_{y1} - V_{y2}, \quad I_z = I_x \tag{1}$$

3. DVCC-Based Biquad

Fig. 3 shows the basic current-mode biquad configuration. The current outputs $I_{o1}(s)$ and $I_{o2}(s)$ are given by:

$$I_{o1}(s) = -\frac{(s^2 + 1/C_1C_2R_2R_3)I_{in1}(s) - (1/C_1R_1)sI_{in2}(s)}{s^2 + (1/C_1R_1)s + 1/C_1C_2R_2R_3} \tag{2}$$

$$I_{o2}(s) = -\frac{-(1/C_1C_2R_2R_3)I_{in1}(s) + (s^2 + (1/C_1R_1)s)I_{in2}(s)}{s^2 + (1/C_1R_1)s + 1/C_1C_2R_2R_3} \tag{3}$$

This circuit enables the LP, BP and BS responses by selection of the input and output currents as follows:

$$T_{LP}(s) = \frac{I_{o2}(s)}{I_{in1}(s)} = \frac{1/C_1C_2R_2R_3}{s^2 + (1/C_1R_1)s + 1/C_1C_2R_2R_3} \tag{4}$$

$$T_{BP}(s) = \frac{I_{o1}(s)}{I_{in2}(s)} = \frac{(1/C_1R_1)s}{s^2 + (1/C_1R_1)s + 1/C_1C_2R_2R_3} \tag{5}$$

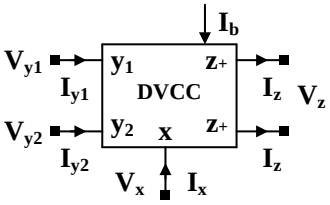

Fig. 1 Symbol for DVCC.

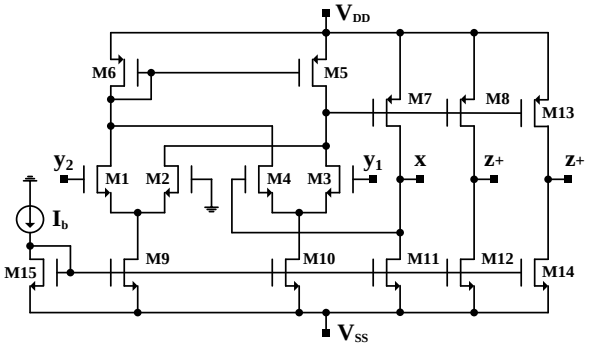

Fig. 2 DVCC with MOS transistors.

$$T_{BS}(s)=\frac{I_{o1}(s)}{I_{in1}(s)}=-\frac{s^2+1/C_1C_2R_2R_3}{s^2+(1/C_1R_1)s+1/C_1C_2R_2R_3} \quad (6)$$

Moreover the HP response can be achieved by the current addition of $I_{HP}(s) = I_{o1}(s) + I_{o2}(s)$, and the AP response is performed selecting the input current $I_{in}(s) = I_{in1}(s) = I_{in2}(s)$. The circuit transfer functions are given as:

$$T_{HP}(s)=\frac{I_{HP}(s)}{I_{in1}(s)}=-\frac{s^2}{s^2+(1/C_1R_1)s+1/C_1C_2R_2R_3} \quad (7)$$

$$T_{AP}(s)=\frac{I_{o1}(s)}{I_{in}(s)}=-\frac{s^2-(1/C_1R_1)s+1/C_1C_2R_2R_3}{s^2+(1/C_1R_1)s+1/C_1C_2R_2R_3} \quad (8)$$

The typical current-mode biquad is consisted of using the basic current-mode one shown in Fig. 4.

The circuit parameters ω_0, Q and H are represented as below:

$$\omega_0=\sqrt{\frac{1}{C_1C_2R_2R_3}},\quad Q=R_1\sqrt{\frac{C_1}{C_2R_2R_3}},\quad H=\frac{R_a}{R_b} \quad (9)$$

The circuit parameters ω_0 and Q can be set orthogonally, and meanwhile the parameter H is able to set independently.

4. A Design Example and Simulation Results

As a design example, we tried to achieve a current-mode biquad with f_0 (= $\omega_0/2\pi$) = 1 MHz, Q = 1.0 and H = 1.0. To realize the specification above, we set that the circuit resistors and capacitors were R_1 = R_2 = R_3 = 12.3 kΩ, R_a = 12 kΩ, R_b = 10 kΩ and C_1 = C_2 = 12 pF, respectively.

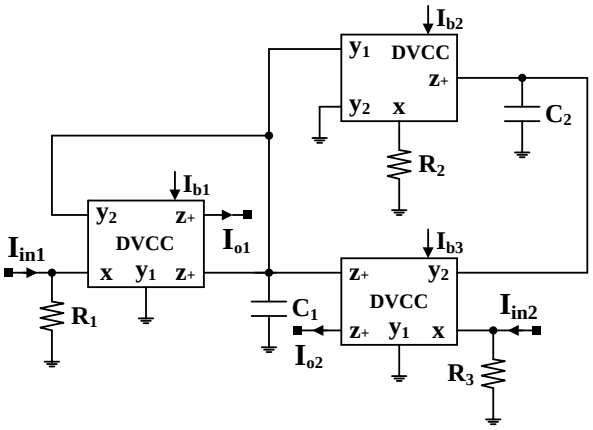

Fig. 3 Basic current-mode biquad.

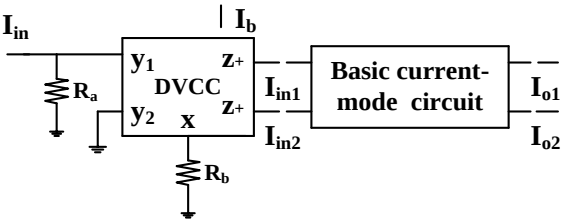

Fig. 4 Typical current-mode biquad.

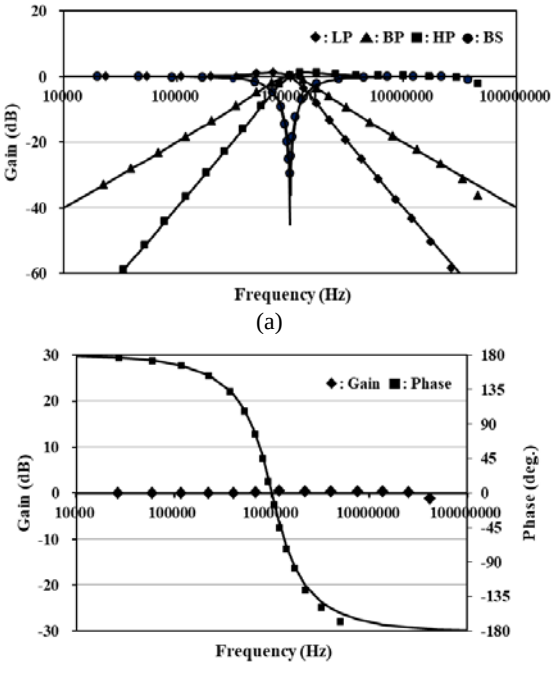

Fig. 5 Simulation responses.

Fig. 5 shows the simulation responses ((a) LP, BP, HP, BS responses, (b) AP response) with PSPICE. In the figures, the marks signify the simulation responses, and the continuous lines show the theoretical ones. This can be viewed as an excellent result. Here we set that the input current, bias currents and DC supply voltages of the DVCCs were I_{in} = 10 μA, I_{b1} = I_{b2} = I_{b3} = I_b = 10 μA and V_{DD} = -V_{SS} = 0.8 V, respectively. The power dissipation was 0.351 mW. In this simulation, the MOS transistor aspect ratios were set as 20 μm/0.5 μm (M1 to M4), 30 μm/2 μm (M5 to M8, M13) and 10 μm/2 μm (M9 to M12, M14, M15). Also we used the device parameters from MOSIS 0.5 μm.

5. Conclusions

This paper has described a novel current-mode biquad employing plus type DVCCs and grounded passive components. The circuit can achieve the standard circuit responses by selecting and/or adding the circuit currents.

The achievement example has been given together with simulation results. The simulation responses were appropriate enough over a wide frequency range. The circuit configuration is very suitable for implementation in CMOS technology.

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