

# Versatile DVCC-Based Current-Mode IAFs without Parasitic Effects

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**Abstract:** This paper introduces current-mode IAFs (inverse active filters) employing DVCCs (differential voltage current conveyors) and grounded passive elements without the parasitic effects. The IAFs enable ILP (inverse low-pass), IBP (inverse band-pass) and IHP (inverse high-pass) responses by adding the circuit current outputs suitably. Additionally the circuit parameters  $\omega_0$  and Q can be set orthogonally adjusting the circuit passive elements. An achievement example is given together with simulation results by PSPICE.

Key words: Analog circuits, IAFs, DVCCs.

## 1. Introduction

Active circuit with high performance has received significant attention. Numerous circuit designs employing active devices such as CCIIs (second generation current conveyors), the DVCCs and so on have been discussed in the literature earlier [1, 2].

An IAF (inverse active filter) has been used to improve the characteristic deterioration in the signal transmission, and applied to the controller in some control systems, etc. Several IAFs with active devices such as FTFNs (four-terminal floating nullors), CFOAs (current feedback operational amplifiers) and the CCIIs have been reported in the past [3-6]. The IAFs [3-5] with the FTFNs and CFOAs used ungrounded passive elements on the device's properties. Moreover a study [6] reported an IBP (inverse band-pass) filter employing the CCIIs. The IAF used the grounded passive elements, and is applied to a PID controller. However as the x-terminal of the CCII is loaded by a capacitor, consequently it leads to improper circuit performance owing to the effect of parasitic resistance at high frequency region.

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The CCII-based and DVCC-based IAFs considering the parasitic effects have not been yet studied sufficiently.

This paper introduces three current-mode IAFs employing the DVCCs and grounded passive elements with the mentioned points above. In the IAFs, all the x-terminals of the DVCCs are grounded through the external resistors considering the parasitic resistors. The filter circuits enable ILP, IBP and IHP responses by suitably adding the circuit current outputs. Additionally the circuit parameters  $\omega_0$  and Q can be set orthogonally according to the circuit passive elements. The voltage-mode IAFs are also presented using basic current-mode ones.

An achievement example is given with PSPICE simulation, and the circuit workability is confirmed.

## 2. DVCC

The symbol of the DVCC is given in Fig. 1, and hereinto it shows dual current output DVCC. The DVCC [2] with MOS transistors is shown in Fig. 2.

The standard DVCC can be characterized by the following terminal equations:

$$V_x = V_{y1} - V_{y2} - I_x R_x, \quad I_z = \pm I_x$$
 (1)

where  $R_x$  shows the parasitic resistance at x-terminal,



Fig. 1 Symbol for DVCC.



Fig. 2 DVCC with MOS transistors.

and the sign  $\pm$  denotes the polarity of the current output  $I_z$  at the z-terminal.

# 3. IAFs and their Performances

Fig. 3 shows basic current-mode IAF circuit configurations. The IAFs are consisted of the DVCCs and grounded passive elements. In these circuits, all the x-terminals of the DVCCs are connected to the grounded resistors considering the parasitic resistances. The filter circuits in Fig. 3 can perform the ILP, IBP and IHP responses by the current addition of  $I_{out}(s) = I_1(s) + I_3(s) + I_4(s)$ .

Fig. 4 shows general current-mode IAF configurations employing the basic current-mode circuit above. The current output  $I_{out}(s)$  is same as the basic current-mode one in Fig. 3.

The circuit transfer functions  $T_{ILP}(s)$  (= $I_{out}(s)/I_{in}(s)$ ),  $T_{IBP}(s)$  and  $T_{IHP}(s)$  are given by:

$$T_{ILP}(s) = \frac{R_a}{R_b} \frac{s^2 + (1/C_1R_3)s + 1/C_1C_2R_2R_4}{1/C_1C_2R_2R_4}$$
(2)

$$T_{IBP}(s) = \frac{R_a}{R_b} \frac{s^2 + (1/C_1R_3)s + 1/C_1C_2R_2R_4}{(1/C_1R_3)s}$$
(3)

$$T_{\rm IHP}(s) = \frac{R_{\rm a}}{R_{\rm b}} \frac{s^2 + (1/C_1R_3)s + 1/C_1C_2R_2R_4}{s^2}$$
(4)

The circuit parameters  $\omega_0$  and Q are represented as

below, respectively:

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_2 R_4}}, \quad Q = R_3 \sqrt{\frac{C_1}{C_2 R_2 R_4}}$$
 (5)

The gain constants  $H_{ILP}$ ,  $H_{IBP}$  and  $H_{IHP}$  are given as:



Fig. 3 Basic current-mode IAF configurations.



Fig. 4 General current-mode IAFs.



Fig. 5 Voltage-mode IAFs.

$$H_{ILP} = \frac{R_b}{R_a}, \quad H_{IBP} = \frac{R_b R_3}{R_a R_2}, \quad H_{IHP} = \frac{R_b}{R_a}$$
 (6)

Thus, the ILP, IBP and IHP responses can be achieved by simple current addition only. Moreover Eqs. (5) and (6) show the circuit parameters  $\omega_0$ , Q can be set orthogonally, and the gain constants  $H_{\text{ILP}}$ ,  $H_{\text{IBP}}$ ,  $H_{\text{IHP}}$  are set independently.

The voltage-mode IAFs are consisted of the basic current-mode ones shown in Fig. 5. Here the voltage output  $V_{out}(s)$  is obtained by converting the current output  $I_{out}$  of the basic current-mode circuit to voltage.

The circuit parameters  $\omega_0$ , Q are same as the current-mode ones, meanwhile the gain constants are given as  $H_{\text{ILP}}=R_a/R_b$ ;  $H_{\text{IBP}}=R_3R_a/R_2R_b$ ; and  $H_{\text{IHP}}=R_a/R_b$ , respectively.

#### 4. A Design Example and Simulation Results

In order to verify our proposal, we tried to realize current-mode ILP and IBP responses using PSPICE simulation program. As a design example, we consider a specification with  $f_0(=\omega_0/2\pi) = 500$  kHz, Q= 1.0 and  $H_{\text{ILP}} = H_{\text{IBP}} = 1.0$ . In the simulation, we have used a macro model of the DVCC shown in Fig. 2.

In accordance with the specification above, we have set the circuit resistors  $R_i$ , capacitors  $C_i$  and bias currents  $I_b$  listed in Table 1. Additionally the input current and power supply voltage were set at  $I_{in} = 10$  $\mu$ A and  $V_{DD} = -V_{SS} = 0.8$  V, respectively.

Fig. 6 shows the simulated ILP and IBP responses. The marks show the simulation responses, meanwhile the solid lines are the theoretical ones. We can find that the simulation responses are favorable enough over a wide range of frequencies. In these circuits, the power dissipations were 0.383 mW and 1.22 mW, respectively.



Fig. 6 Simulation responses.

Table 1 Circuit element values.

х	ILP	IBP	
$R_I$	0.1 kΩ	20 kΩ	
$R_2$	15 kΩ	20 kΩ	
$R_3$	15 kΩ	20 kΩ	
$R_4$	15 kΩ	20 kΩ	
$R_a$	10 kΩ	10 kΩ	
$R_b$	10 kΩ	10 kΩ	
$C_{I}$	20 pF	16 pF	
$C_2$	20 pF	16 pF	
$I_b$	10 µA	36 µA	

MOS transistor	W/L	
M1-4	20 μm/0.5 μm	
M5-8, M13	30 μm/2 μm	
M9-12, M14-15	10 μm/2 μm	

Table 2 MOS transistor aspect ratios.

In this simulation, the aspect ratios of MOS transistors are listed in Table 2. Also we have used the parameters obtained from MOSIS 0.5  $\mu$ m for other device parameters.

### **5.** Conclusions

In this paper, we have proposed versatile DVCC-based three current-mode IAFs. The IAFs use the grounded resistors at all the x-terminals of the DVCCs reducing the parasitic effects. We have demonstrated that the filter circuits enable ILP, IBP and IHP responses by suitable addition of the circuit current outputs. Additionally the circuit parameters  $\omega_0$  and Q can be set orthogonally adjusting the circuit passive elements. Furthermore the voltage-mode IAF configurations have been introduced employing the basic current-mode ones.

The achievement example has been given together with simulation results by PSPICE. The simulation

responses have been appropriate enough over a wide frequency range.

The non-idealities (i.e. voltage and current tracking errors) of the DVCC affect the circuit performances. The solution for this will be discussed in the future.

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