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Nonlinear Modelling of Automatic Gain Control Loops Considering Loop Dynamics and Stability

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Abstract: This work presents modelling aspects of automatic gain control (AGC) loops based on linear-in-dB variable gain amplifiers (VGAs). In these loops, the VGA control voltage is also an excellent received signal strength indicator (RSSI). The VGA gain is however nonlinearly related to the control voltage. Moreover, VGAs and detectors undergo nonlinear compression under high input amplitudes during settling transients. The main contribution in this work is a proposed nonlinear model based on simple and readily available components from the "*analogLib*" and "*functional*" libraries in CADENCE design environment -making it very easy and fast to build and simulate- that captures the nonlinear effects of AGC loops. The model is capable of verifying the AGC loop stability and capturing the loop dynamics with high accuracy compared to time consuming circuit level simulations. This provides insights into system level parameters such as AGC loop bandwidth, phase margin, settling time as well as estimating the AGC range and RSSI voltage vs. input power. Measurement results from a fabricated AGC prototype are in good agreement with simulation and modelling results thus validating the proposed modelling approach.

Key words: Amplifiers, detectors, feedback circuits, gain control, integrated circuit modelling.

1. Introduction

Automatic gain control loops are used in many systems to stabilize the signal level before analog-to-digital conversion [1-3]. A typical AGC loop is shown in Fig. 1. As the input signal level changes, the detector output (Vdet) changes accordingly, this Vdet is compared with a reference voltage (Vset) that defines the desired output level and the resulting error is filtered by a loop integrator and fed as the VGA control voltage (Vc) to counteract the input level variations.

Linear-in-dB VGAs in particular are favorable because they additionally provide for an excellent RSSI [1] beside leading to a constant settling time of AGC loops [2]. Simple mathematical models describing these loops are derived in Refs. [2, 3] under various small signal assumptions to linearize and simplify the problem, but for most practical cases, simulations are used to investigate the large signal behavior which would otherwise be so complicated to solve analytically [1-3].

In this work, a nonlinear model is proposed based on readily available components from the "*analogLib*" and "*functional*" libraries in CADENCE design environment making it very easy and fast to build and simulate thus providing insights into the AGC system level parameters.

This article is an extended version of a previous conference-proceeding publication [4]. With respect to the first version, more insights on the relations between the ACG loop circuit design and the main model parameters are presented. Moreover, the model is investigated for validity in situations where the AGC loop is unstable. The remainder of this article is organized

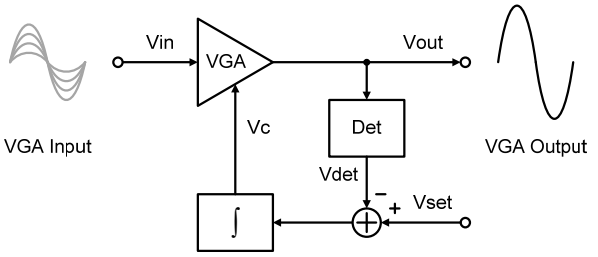

Fig. 1 AGC loop block diagram.

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as follows: In section 2, the models for the AGC building blocks are introduced and the estimation of the main model parameters from the circuit design is discussed. Simulation results of the proposed model are presented in section 3. Then in section 4, measurements from a fabricated baseband AGC loop for frequency modulated continuous wave radar applications are discussed. Finally, the results from this work are concluded in section 5.

2. AGC Loop Design and Modelling

2.1 Variable Gain Amplifier Design

A linear-in-dB VGA has a gain vs. Vc characteristic that ideally follows the relation

$$A_{VGA} = S_{VGA}\frac{\mathrm{dB}}{\mathrm{V}} \times \mathrm{Vc} + A_{VGA\_0}\mathrm{dB} \qquad (1)$$

where S_{VGA} is the slope of the linear-in-dB gain characteristics and A_{VGA_0} is the gain at Vc = 0.

In this work, the VGA is implemented based on the gain-interpolating architecture shown in Fig. 2 due to its excellent linear-in-dB gain characteristics [5]. It is composed of an R-2R ladder providing 6 dB of attenuation per section followed by a fixed gain amplifier where the overall gain depends on the selected tap of the ladder. In order to achieve intermediate gain levels between the 6 dB steps, the outputs from the ladder are weighted (by means of trans-conductor stages with weighted bias currents as shown in Fig. 2) and added before passing through the amplifier to perform an interpolation operation.

For achieving the linear-in-dB gain characteristic with a low log conformance error, a Gaussian interpolator is used as shown in Fig. 2 [5] where bipolar transistors Q1-Q8 generate partially overlapping Gaussian shaped currents at their outputs vs. a linear change in the differential control voltage (Vcp-Vcn) as shown in Fig. 3. The derivation of S_{VGA} based on the VGA circuit design parameters can be explained in two steps: First: Determine the amount of control voltage needed to switch from one tap of the attenuator ladder to the other; Second: Divide the attenuation per section by this amount to obtain S_{VGA} in dB/V. The first step is explained by means of the voltage and current distributions on the interpolator's resistor string as shown in Fig. 4.

When Vcp = Vcn, the I_b currents are ideally split in the R_b resistors as shown in the top part of Fig. 4 where the potential distribution is indicated by the size and height of the solder dots. It is clear that the bases of Q4 and Q5 have the highest potential in this case and thus Q4 and Q5 share almost all of I_e equally. This corresponds to point A in Fig. 3.

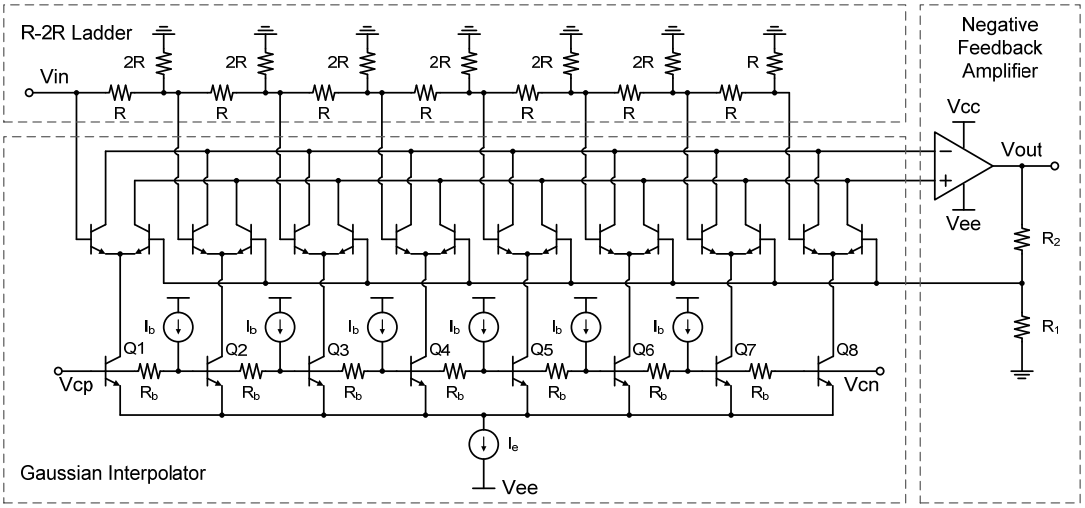

Fig. 2 Gain interpolating VGA architecture proposed in Ref. [5].

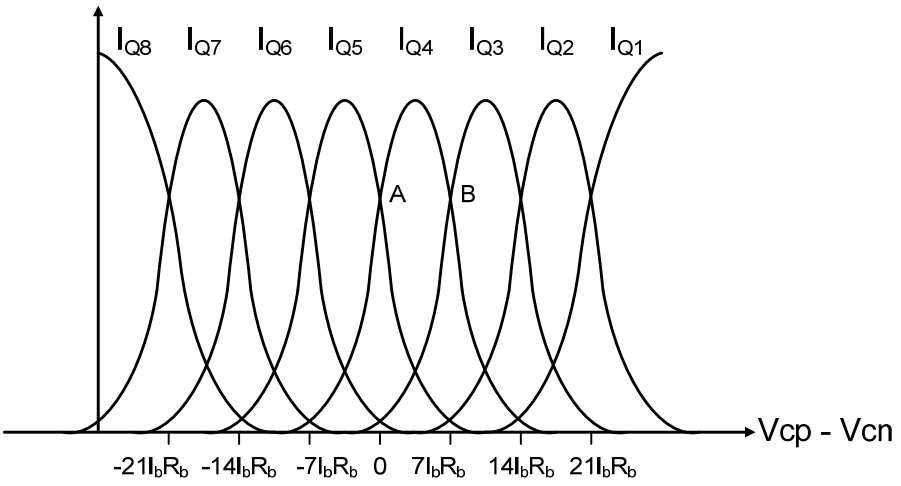

Fig. 3 Gaussian interpolator output currents.

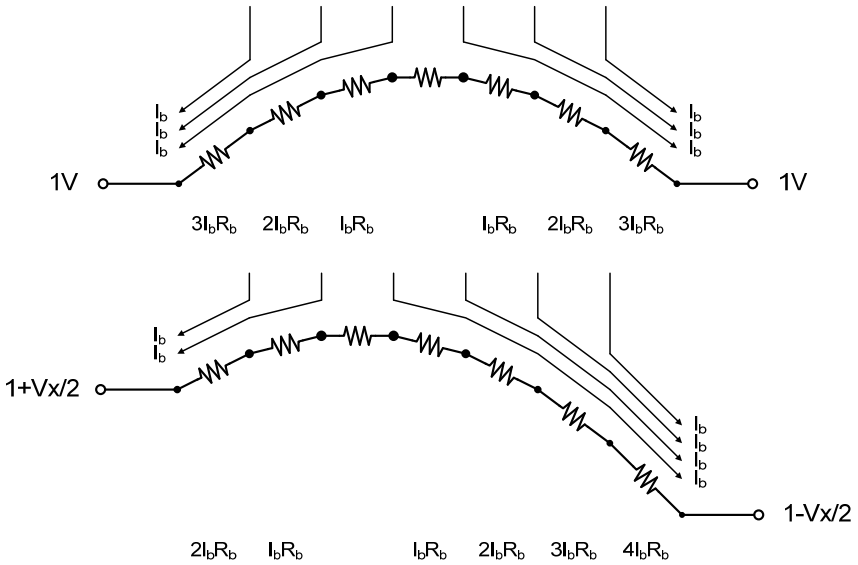

Fig. 4 Potential distribution on the Gaussian interpolator resistor string.

To move from point A to point B in Fig. 3, a differential control voltage Vx is needed to raise the potential of the bases of Q3 and Q4 sliding only $2I_b$ to the left side and sliding $4I_b$ to the right side. Now it can be observed by applying KVL that the voltage Vx that is needed to steer the bias current from one trans-conductor stage to the other is equal to $7I_bR_b$.

This is a good feature of this architecture because the value of I_bR_b could be well controlled in integrated designs using a poly current reference with the same resistor type of R_b. This leads to low S_{VGA} variations over process, voltage and temperature (PVT).

For this eight tap VGA design, I_b = 10 μA and R_b = 8 kΩ thus needing 0.56 V of differential control voltage for steering the bias current from one trans-conductor stage to the other.

This means a total of 3.92 V to steer the current from the first to the eighth trans-conductor stage. Since a single ended control voltage is desirable, an inverting amplifier is used to generate Vcn from Vcp using a 1 V reference Vc_pivot as shown in Fig. 5. This way, when Vc_scaled changes from 0-2 V, Vcp also changes from 0-2 V while Vcn changes from 2-0 V.

Therefore, the value of the control voltage needed to steer the bias current from one trans-conductor stage to the other (ΔVc) is given by:

$$\Delta Vc = \frac{7 I_b R_b}{2} = \frac{7 \times 10\ \mu A \times 8\ k\Omega}{2} = 0.28\ \text{V} \quad (2)$$

where the division by two is to account for the fact that ΔVc is the single ended control voltage change.

The maximum voltage level of 2 V at the bases of Q1-Q8 ensures that their base-collector junctions are always reverse biased thus preventing undesired sneak current paths on the interpolator resistor string.

However, with the supply voltage in this work being 3 V, when the AGC loop gets a very low or no input, it will keep trying to increase the VGA gain by increasing Vc all the way up to the supply. While this would lead to an undesired forward biasing of the base collector junction of Q1 in the interpolator, a more important effect would be that when a large input signal is then introduced, the loop will waste some time to bring Vc down from 3 V to 2 V after which the VGA gain starts to actually change vs. Vc. To alleviate this issue, a 3:2 potential divider is used to extend the valid control voltage range to cover the full headroom of 3 V as shown in Fig. 5 [1]. This would change Eq. (2) to be:

$$\Delta Vc = \frac{7 \times 10\ \mu A \times 8\ k\Omega}{2} \frac{3}{2} = 0.42\ \text{V} \quad (3)$$

Finally, noting that an R-R ladder rather than an R-2R ladder is used [6], the attenuation per section is not 6 dB. Rather it can be calculated under the infinite R-R ladder assumption as shown in Fig. 6.

For an infinite R-R ladder, removing one section would not change the value of the input resistance (R_{in}). Therefore R_{in} can be calculated as:

$$R_{in} = R + R \,//\, R_{in} \quad (4)$$

Solving Eq. (4) for R_{in}, it is found to be equal to $(1+\sqrt{5})/2 \approx 1.618$ R which in mathematics is called the golden ratio [7]. In practice, the ladder is not infinite so the last section has to be an R-0.618R to satisfy the infinite ladder assumption.

With these assumptions, the attenuation per section (ΔAtt) can be calculated as:

$$\Delta Att = -20 log\left(\frac{R \,//\, R_{in}}{R + R \,//\, R_{in}}\right) \approx 8.36\ dB \quad (5)$$

which leads to a wider VGA dynamic range for the same number of attenuator ladder sections [5]. Note that for layout purposes, the last section is an R-0.5R section as an approximation to make it more convenient when use identical resistor units to layout the R and 0.5R resistors with very good matching [6].

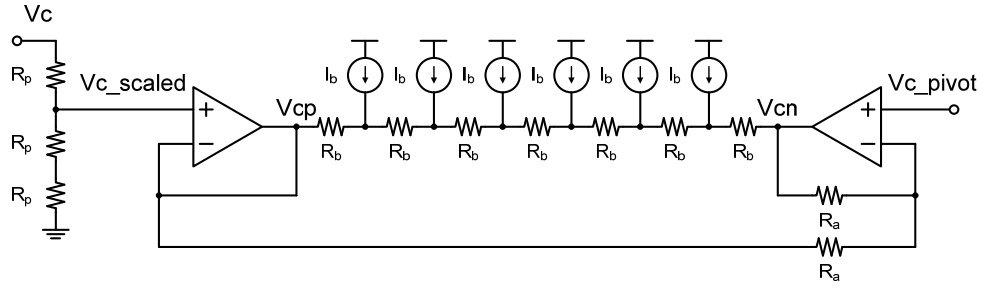

Fig. 5 Generating Vcp and Vcn from the external control voltage Vc.

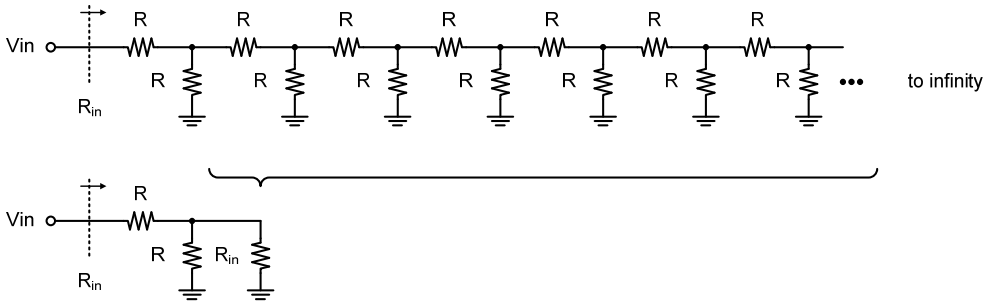

Fig. 6 R-R attenuator ladder analysis.

Now from Eqs. (3) and (5), S_{VGA} can be estimated as:

$$S_{VGA} = \frac{\Delta Att}{\Delta Vc} = \frac{8.36\ \text{dB}}{0.42\ \text{V}} \approx 20\ \text{dB/V} \qquad (6)$$

2.2 Variable Gain Amplifier Modelling

In order to build a model for Vout as a function of Vin and Vc, Eq. (1) is rearranged to:

$$\text{Vout} = \text{Vin} \times 10^{\frac{S_{VGA}\frac{\text{dB}}{\text{V}} \times \text{Vc} + A_{VGA\_0}\text{dB}}{20}} \qquad (7)$$

A simple model for this nonlinear function is proposed as shown in Fig. 7. For fast simulations, only the amplitude levels are considered, modelling them as dc voltage values [4]. This is similar to an envelope simulation where the envelope of the signal is the main concern rather than the instantaneous voltage levels in the carrier. This leads to a significant reduction in the simulation time.

The model is built on three steps: first, the exponent term in Eq. (7) is obtained using a voltage controlled voltage source (*vcvs*) and a dc source (*vdc*) from the "*analogLib*" library.

Second, in order to perform the 10^X operation, its inverse $\log_{10}X$ operation is used in a feedback loop. This is because only a logarithmic amplifier (*logAmp*) is available in the "*functional*" library. But it has to be noted that the *logAmp* is a natural logarithmic amplifier i.e. it actually performs a $\log_e X$ operation. And since $\log_{10}X = \log_e X/\log_e 10$, therefore $\log_{10}X$ can be obtained by using a *vcvs* with a gain of 1/ln(10) after the *logAmp* [8].

In order to avoid introducing negative values to the *logAmp* during the initial iterations of the transient or dc solver, the minimum output voltage of the *vcvs* used as the amplifier in the feedback loop is set to 0 as shown in Fig. 7.

Finally, the result which now represents the VGA gain is multiplied by Vin using a *multiplier* from the "*functional*" library followed by a unity gain *vcvs* with a maximum output voltage of the supply (Vdd) in order to additionally capture the effect of VGA output compression which means that the output amplitude from the VGA could not exceed the supply voltage.

In this work, the model is used to mimic the VGA design in Ref. [6] with S_{VGA} = 20 dB/V and A_{VGA_0} = -1 dB as shown in Fig. 8.

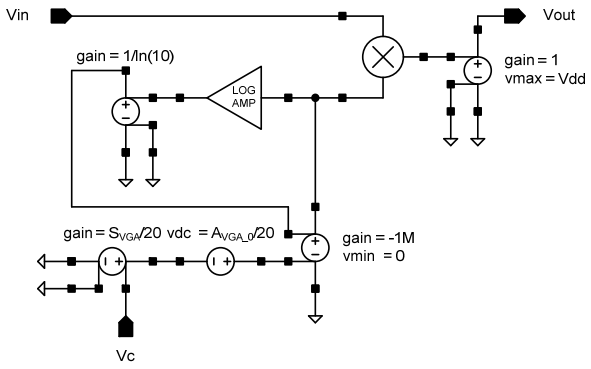

Fig. 7 Linear-in-dB VGA model.

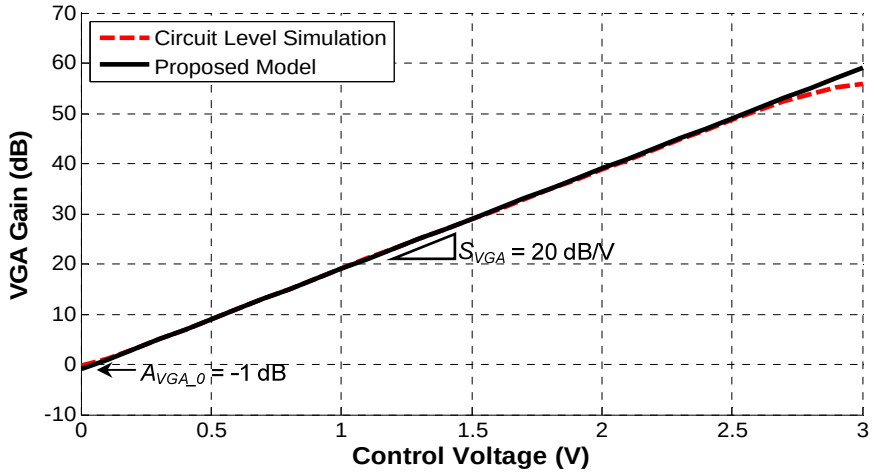

Fig. 8 Linear-in-dB VGA characteristics curve fitting.

2.3 Detector Design

An accurate mean absolute law detector architecture [9] has been designed for the use in this work as shown in Fig. 9. Transistors M1-M8 form a V-to-I half wave rectifier. Together with transistors M9-M16 where the input signal is swapped, a full wave rectifier is obtained. The resistors R_{deg} increase the linear range of the V-to-I conversion. For the widest detector input dynamic range, R_{deg} is chosen as the highest value that keeps M1, M2, M9 and M10 in saturation region.

The AC components of the rectified current flow in the large filtering capacitor C_{filt} while the DC component flows into the I-to-V converter composed of M17-M22 leading to a differential voltage at the drains of M19 and M20 that is equal to the mean absolute value of the differential input signal. In order to define the output common mode, a common mode feedback (CMFB) loop is used comprising sensing resistors R_{sense}, amplifier M23-M27 and compensation capacitors C_{comp} for common mode stability.

Designing the I-to-V converter core (M17-M20) as a replica of the rectifier core (M1-M4 and M9-M12) leads to an inherent cancellation of PVT variations which leads to an accurate detector design without the need for complex calibration schemes [9].

For immunity against part-to-part variations due to random mismatches, the entire detector core components of Fig. 9 are designed as pairs such that they can all be matched together using common centroid layout matching techniques.

The detector sensitivity (S_{DET}) which is defined as the slope of the detector input/output characteristics can be calculated for a sinusoidal input with a differential amplitude (A_{peak}) and a frequency (f_D) as:

$$S_{DET} = \frac{\frac{1}{T_D}\int_0^{T_D}\left|A_{peak}\sin\left(2\pi f_D t\right)\right|dt}{A_{peak}} = \frac{2}{\pi}\ \text{V/V} \qquad (8)$$

where T_D is the period which is equal to $1/f_D$. Therefore Eq. (8) suggests that S_{DET} is approximately equal to 0.64 V/V.

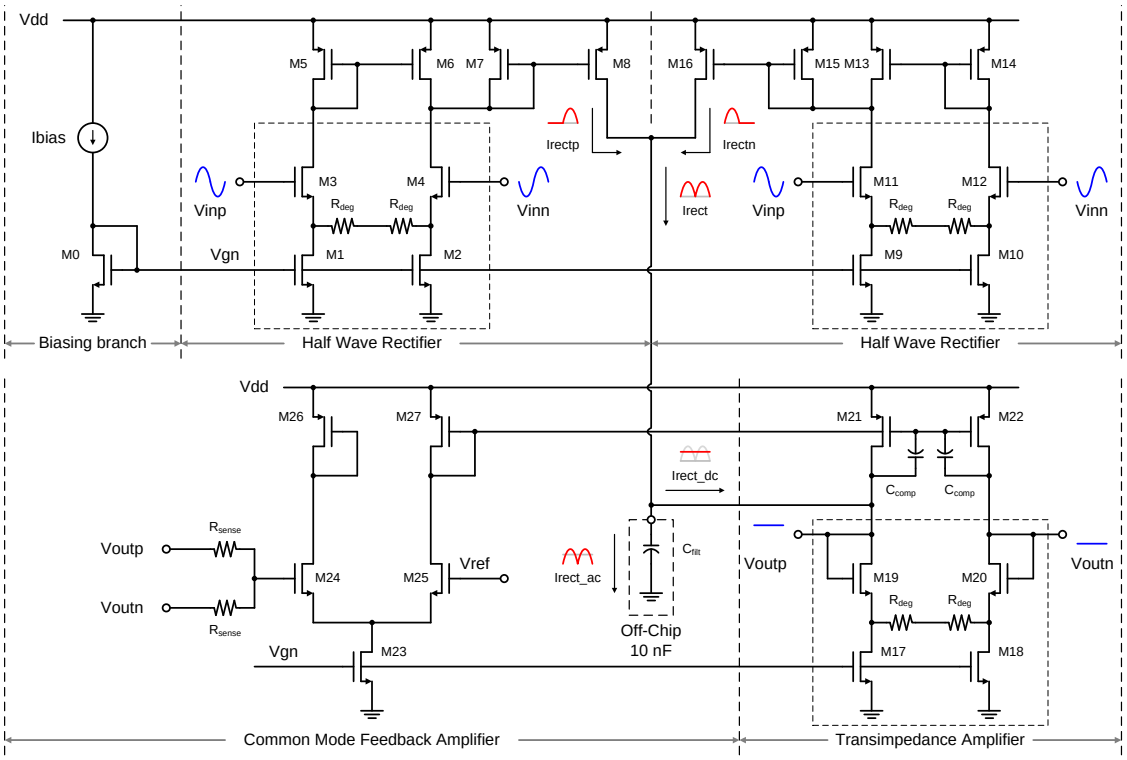

Fig. 9 Mean absolute law detector core schematic.

2.4 Detector Modelling

The detector is simply modelled by a *vcvs* with a gain of S_{DET1} to model the detector sensitivity. In order to capture detector compression under large signal drive, the maximum output voltage of this *vcvs* is set to S_{DET1} multiplied by a certain input knee voltage (V_k). Additionally a second *vcvs* can be used as shown in Fig. 10 to capture a reduced detector sensitivity for input amplitudes beyond V_k as shown in Fig. 11 where S_{DET1} = 0.64 V/V, S_{DET2} = 0.2 V/V and V_k = 1.7 V. To ensure that the second *vcvs* kicks in only after V_k, its negative terminal is connected to a dc voltage of V_k and its minimum output voltage is set to 0 V.

In simple analytical models [2, 3], Vdet is assumed to instantaneously follow the VGA output amplitude to simplify the analysis. However, practically there is a delay introduced by the detector pole that may affect the AGC loop stability [1]. This effect is captured in this model by introducing a pole composed of R_{det}, C_{det} and a unity gain *vcvs* as shown in Fig. 10. In this work, R_{det} and C_{det} can be extracted from the detector design in Fig. 9 where R_{det} is equal to $R_{deg} + 1/g_{m,\ M19}$ which is approximately equal to R_{deg} = 10 kΩ while C_{det} is equal to C_{filt} = 10 nF.

2.5 Loop Integrator Modelling

To close the AGC loop, the loop integrator is modelled by a *vcvs* as the negative feedback amplifier where the error between Vdet and Vset is integrated to generate Vc as shown in Fig. 12. The maximum output voltage of the *vcvs* is set also to Vdd to mimic the practical case. Note that R_{comp} is used to introduce a zero at $2\pi R_{comp}C_{intg}$ in the AGC loop to cancel the pole at $2\pi R_{det}C_{det}$ introduced by the detector [1].

In this design, R_{comp} = 10 kΩ, R_{intg} = 100 kΩ and C_{intg} = 10 nF. Based on all the chosen design parameters in this work, the small signal AGC loop bandwidth can be estimated as: [1]

$$f_{BW\_AGC} \approx \frac{S_{VGA}\frac{\text{dB}}{\text{V}} \times S_{DET1}\frac{\text{V}}{\text{dB}}}{2\pi R_{intg}C_{intg}} \approx 230 \text{ Hz} \qquad (9)$$

This translates to an AGC settling time to within 5% i.e. 0.5 dB of the final value in response to an input amplitude step within three time constants (3τ) of $3/(2\pi f_{BW\_AGC}) \approx 2$ msec.

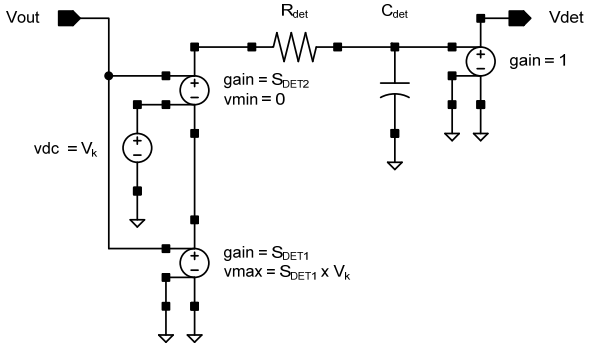

Fig. 10 Detector model.

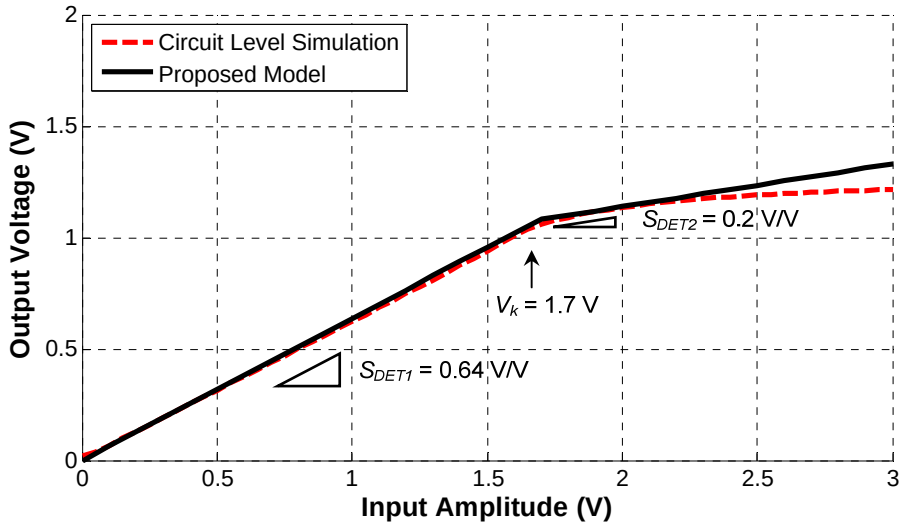

Fig. 11 Detector characteristics curve fitting.

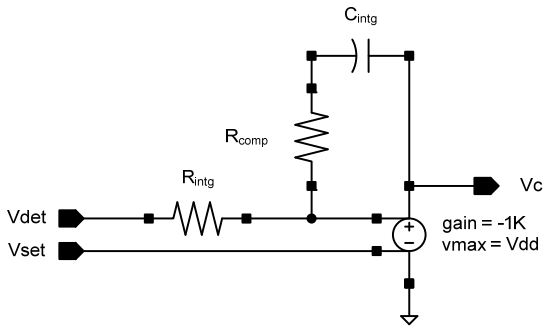

Fig. 12 Loop integrator model.

3. Simulation Results

Connecting the blocks together as shown in Fig. 13, the AGC model is built. The first benefit of this model is that the AGC loop stability can be verified quickly using a stability analysis by introducing a stability probe in the path of Vc.

Such an analysis was not possible using the circuit level of the AGC loop because the stability analysis is a linear small signal analysis while the detector's operation relies on nonlinear large signal behaviour.

The AGC loop gain and phase plots from this analysis are shown in Fig. 14. It can be seen that due to the proper choice of R_{comp}, the detector pole is cancelled and the AGC loop is reduced to an unconditionally stable single pole loop with a phase margin of 90° at a loop bandwidth of around 230 Hz as expected.

The second benefit of the model is that it quickly captures the transient loop dynamics with very good accuracy compared to full circuit level simulations as shown in Fig. 15. The model has the advantage of a fast simulation time of less than one second compared to full circuit level simulation which takes around three hours even with high performance simulation mode enabled using eight threads on eight cores.

This comes in handy to first provide insights into the design and give a good estimate of the loop dynamics before verification simulations are run. For

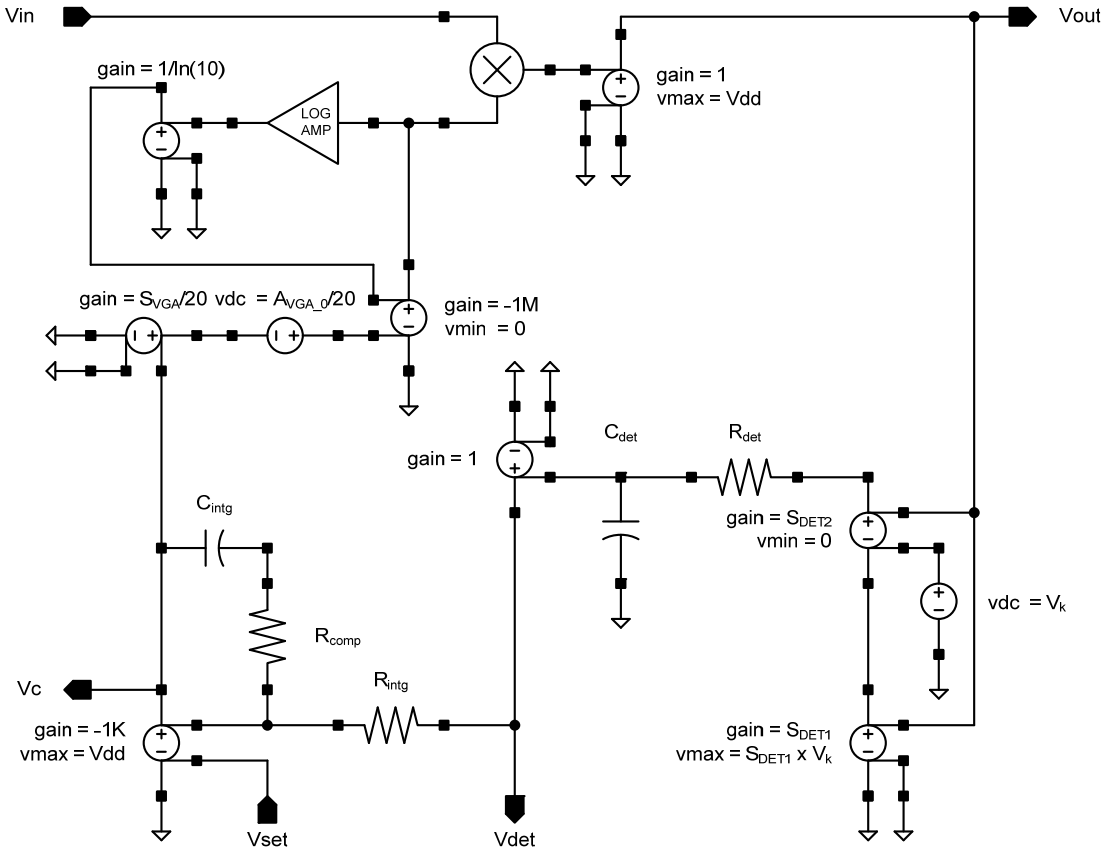

Fig. 13 Full AGC loop model.

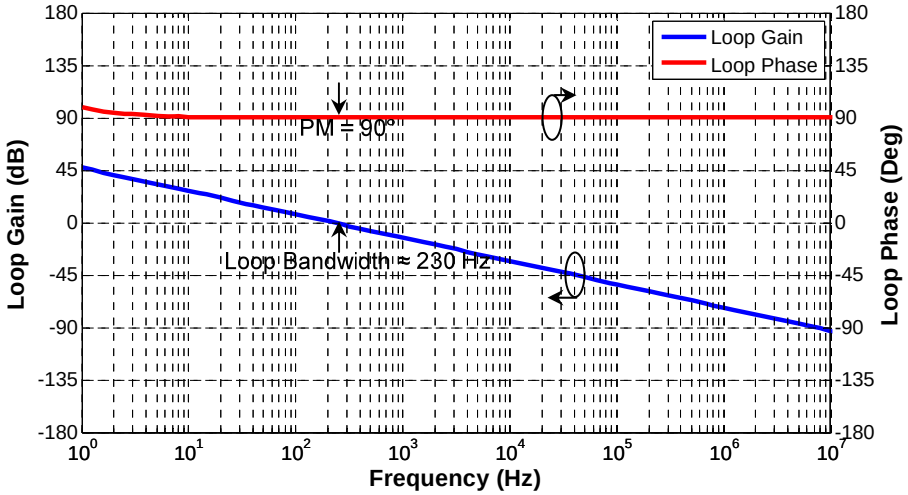

Fig. 14 Simulated AGC loop gain and phase using stability analysis.

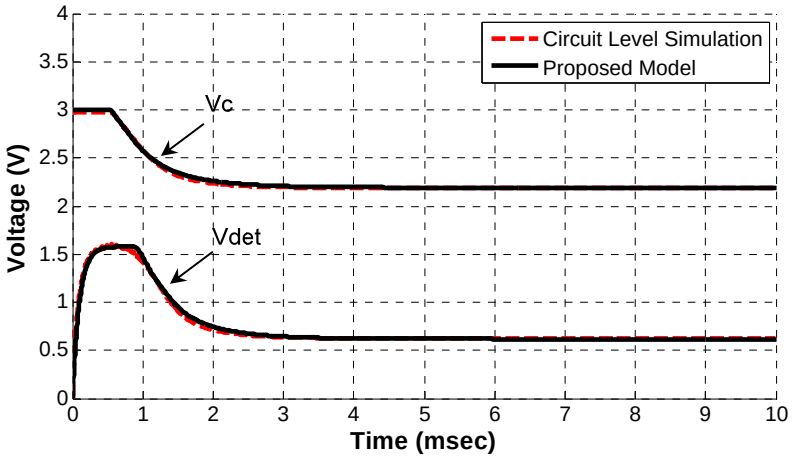

Fig. 15 Simulated vs. modelled AGC loop dynamics.

example, bad choices of the design parameters can lead to low AGC loop phase margin and consequently the loop dynamics involve excessive ringing as can be seen from the example in Fig. 16 where the loop has a phase margin of only 20° and the model still captures the loop dynamics with very good accuracy.

Furthermore, very bad choices of the design parameters can lead to oscillations in case of zero or negative phase margins. This can still be captured by the model as can be seen from the example in Fig. 17.

In this particular case, the circuit level simulation lasted for more than six hours due to the instability while the model still runs in under one second.

To further demonstrate the advantages of this fast simulation model, the settling time of the loop is evaluated for different possible values of input power levels introduced to the VGA's 100 Ω differential input impedance. In this scenario, similar to the previous loop dynamics simulation, the input power is at first disabled and thus the AGC loop starts with Vc at 3 V (maximum gain). Then the input is enabled and the AGC loop starts to regulate the output to the desired amplitude of 0 dBV (the output is expressed in dBV rather than dBm units because the VGA is designed to drive capacitive loads).

The next step occurs at 10 msec where the input is reduced by 6 dB and the AGC loop starts to respond to bring the output back to 0 dBV. The simulation is repeated multiple times each with a different initial power level in the range from –40 to +10 dBm.

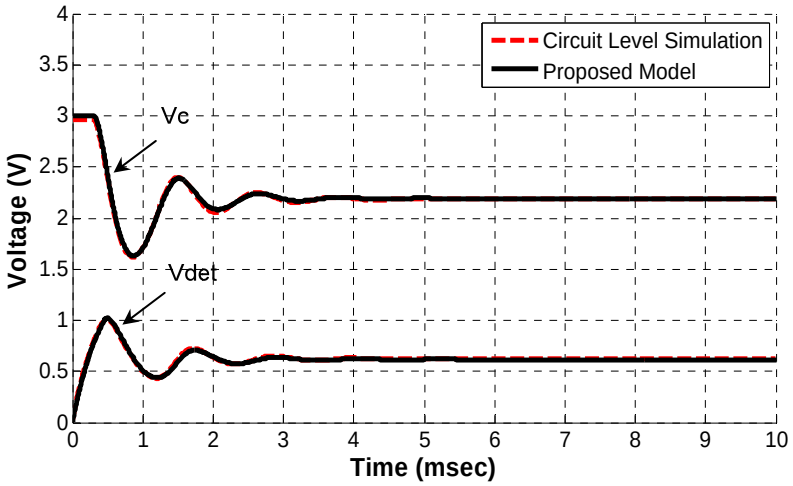

Fig. 16 Simulated vs. modelled AGC loop dynamics with low phase margin.

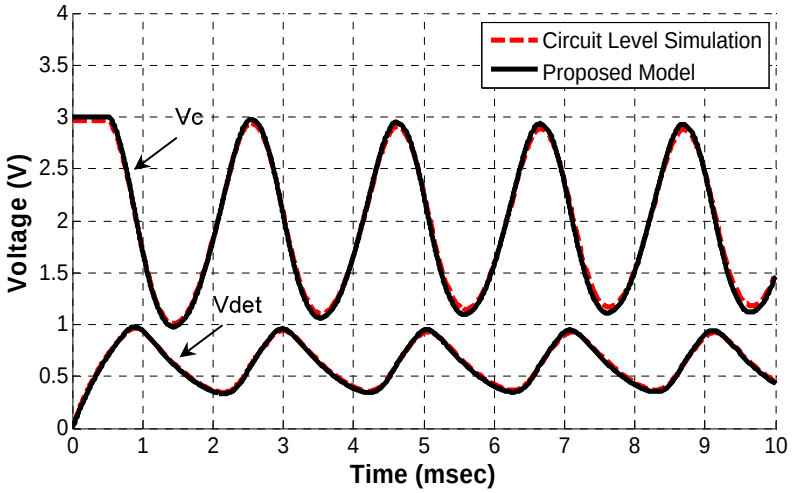

Fig. 17 Simulated vs. modelled AGC loop dynamics with negative phase margin.

It can be seen from the results in Fig. 18, that the second settling time is always constant at around 2 msec as expected from the small signal analysis. However, this is not the case for the initial acquisition which is basically a nonlinear settling because the VGA spends some time in compression driving the loop integrator to reduce Vc linearly (not to be confused with linear settling where Vc is controlled exponentially) for some time that is dependent on the input power level. This behaviour is well captured by the model and thus lends itself to easily determining system level specifications for the required preamble time to guarantee that the AGC loop is settled. In this design, this preamble time is found to be equal to 5 msec for the worst case of 10 dBm input.

4. Measurement Results

In order to validate the proposed modelling procedure, the designed AGC loop has been fabricated on an IBM 0.18 µm BiCMOS technology. The chip layout and die photo are shown in Fig. 19. The chip has an area of 0.72 mm^2 including pads. The measurement setup is shown in Fig. 20. The input is supplied using a R&S SMBV100A signal generator while the output is measured using an Agilent MSO6034A digital storage oscilloscope. MATLAB scripts have been developed to automate the measurement instruments to speed up the measurement process.

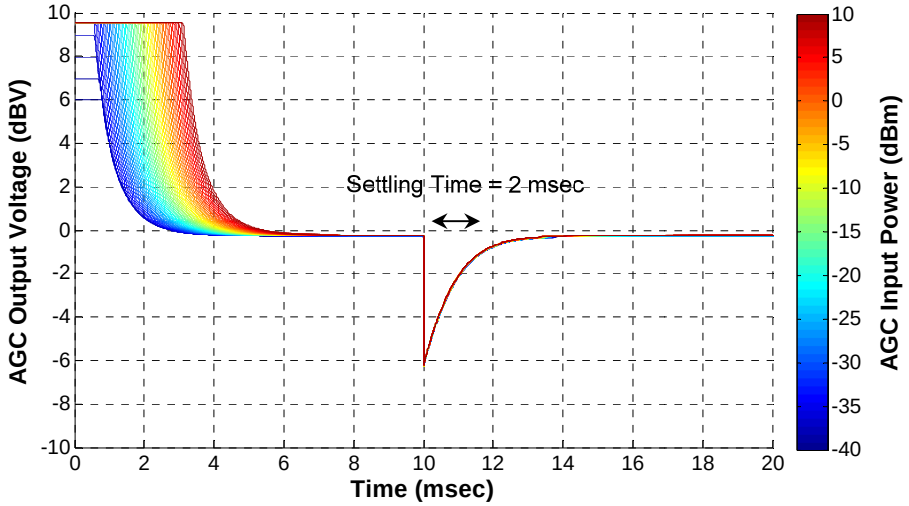

Fig. 18 Modelled AGC settling time vs. input power in dBm.

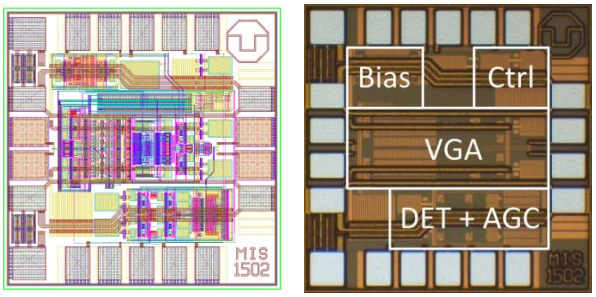

Fig. 19 Chip layout and die photo.

Fig. 20 AGC loop measurement setup.

Fig. 21 shows that the fabricated AGC loop is stable with good agreement between the measured, simulated and modelled loop dynamics.

Moreover, Fig. 22 shows that the AGC could track changes in the input power in the range from –44 to +11 dBm introduced to the VGA's 100 Ω differential input impedance beyond which the AGC loop could not track anymore and the VGA output follows its input in a dB-by-dB behaviour.

The proposed model can also be used to capture this behaviour using a simple dc sweep of the input level and recording the dc values of Vc and Vout (which now represents the final values after the loop has settled during the iterations of the dc solver) as shown in Fig. 22. The slight discrepancy at the low input levels is due to the curve fitting error between the simulated and modelled VGA at the higher gain settings as can be seen from Fig. 8. But the model is still sufficient to quickly get a first order approximation on the expected Vc vs. input power which can serve as an excellent RSSI [1].

If a better back-fitting is desired, the integrator's *vcvs* maximum output voltage in Fig. 12 may be reduced from Vdd by 0.25 V to reduce the useful dynamic range of the VGA which is currently 20 dB/V × 3 V = 60 dB by 5 dB to better match the measured VGA dynamic range of around 55 dB.

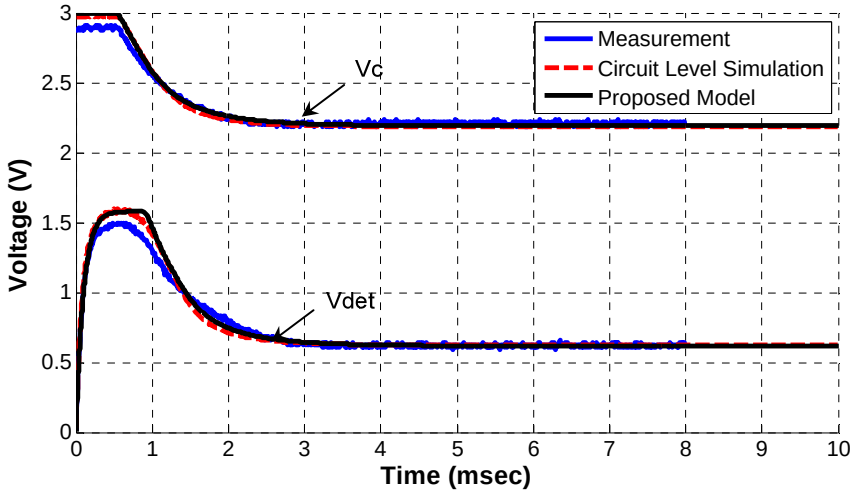

Fig. 21 Measured vs. simulated vs. modelled AGC loop dynamics.

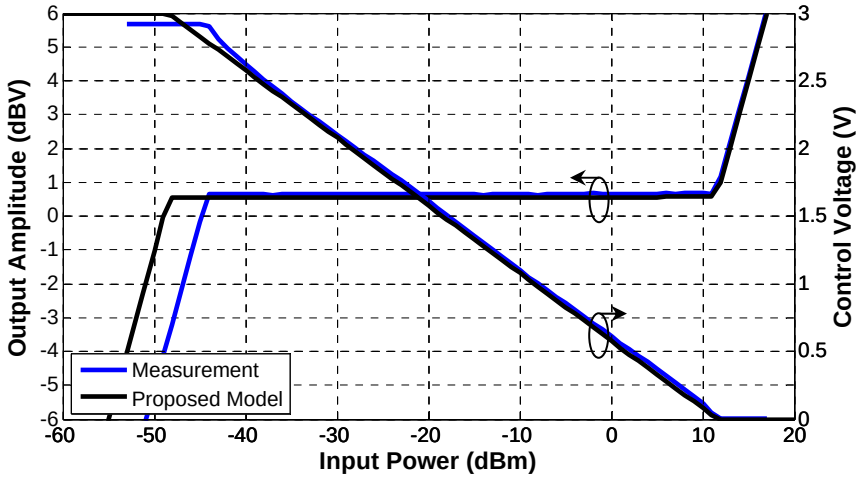

Fig. 22 Measured vs. modelled VGA output and Vc vs. input power.

5. Conclusion

A nonlinear model of AGC loops has been presented. The model relies on simple and readily available components from the "*analogLib*" and "*functional*" libraries in CADENCE making it very easy and fast to build and simulate.

The model is capable of verifying the AGC loop stability and capturing the loop dynamics with high accuracy compared to time consuming full circuit level simulations. The model provides insights into system level parameters such as AGC loop bandwidth, phase margin, settling time as well as estimating the AGC range and RSSI voltage vs. input power.

Measurement results from a fabricated AGC prototype are in good agreement with circuit level simulation and modelling results thus validating the proposed modelling procedure.

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