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Estimating the Limits in System Design for 48 V Automotive Power Applications

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Abstract: The design process in power electronics is driven by increased utilisation level of the used components to gain performance whilst keeping cost low. This article provides an overview on challenges in low-voltage high-current systems, e.g. used in automotive applications. The main content points are: topology selection—single systems vs. cascaded systems, PCB manufacturing technology overview, current measurement methods, bulk capacitor design (ceramic DC link) and PCB design instructions for high-current systems. The PCB design instructions target on optimised thermal design for maximised PCB utilisation and on optimised track design for a low inductance DC link interconnection. The paper bases on calculations, measurements and simulations.

Key words: High current application, 48V system, DC link optimization, PCB optimization, current carrying capability.

1. Introduction

Today's power electronic systems become more complex and the utilisation level of the components, like semiconductors, chokes, capacitors and the PCB should be increased to reduce system cost in respect to rated power. To enhance the component utilisation the system design has to be adapted to the application. Influencing factors for system design are summarised in Fig. 1. The key issues are: efficiency, power density, design space, ambient temperature, reliability and system costs.

This contribution focuses on the challenges in low-voltage, high-current systems. Main application is the automotive sector with 12 V, 24 V or 48 V system voltage. Typical applications are electrical turbocharger, ancillary components and electric pumps. A system voltage below 60 V_{DC} (safety extra-low voltage level) is easy to handle, because there are no additional safety arrangements necessary. The technical challenges in low-voltage, high-current systems are versatile: topology selection, choice of the PCB manufacturing technology, optimised PCB layout to push the thermal limits, system modelling under thermal limiting conditions, high-current measurement solutions and especially low impedance DC link interconnection. This article will highlight the challenges and deliver solutions in low-voltage, high-current systems.

Corresponding author: Ulf Schwalbe, Dr., research fields: power electronics and control, switch mode power supplies, power semiconductor application.

2. Challenges in System Design

2.1 Topology Selection

The topology selection is the first step in system design. There are versatile possibilities: classical single converter, serial cascades systems and parallel cascaded systems also known as interleaved systems (Fig. 2). This paragraph shows a system comparison for an inverter with P_{EL} = 25 kW, V_{IN} = 48 V applied in a modular driving system. A comparison of three systems, classical approach (one inverter @ 48 V battery voltage), serial cascaded system (four inverters @ 200 V battery voltage) and parallel cascaded system (four inverters @ 48 V battery voltage) was done analytically with a simplified inverter model [7]. The calculation was verified by measurements in the parallel cascaded system.

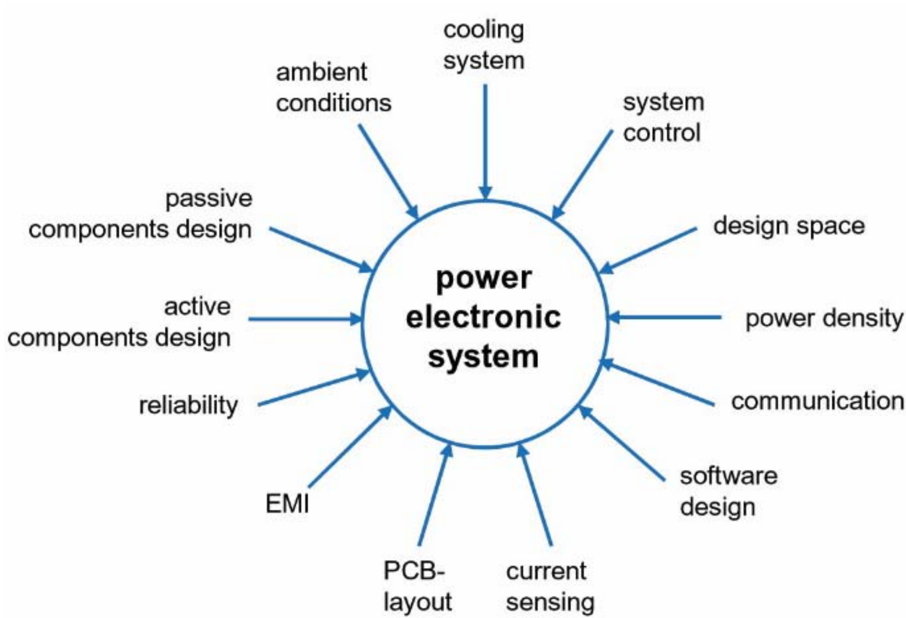

Fig. 1 System design influencing factors.

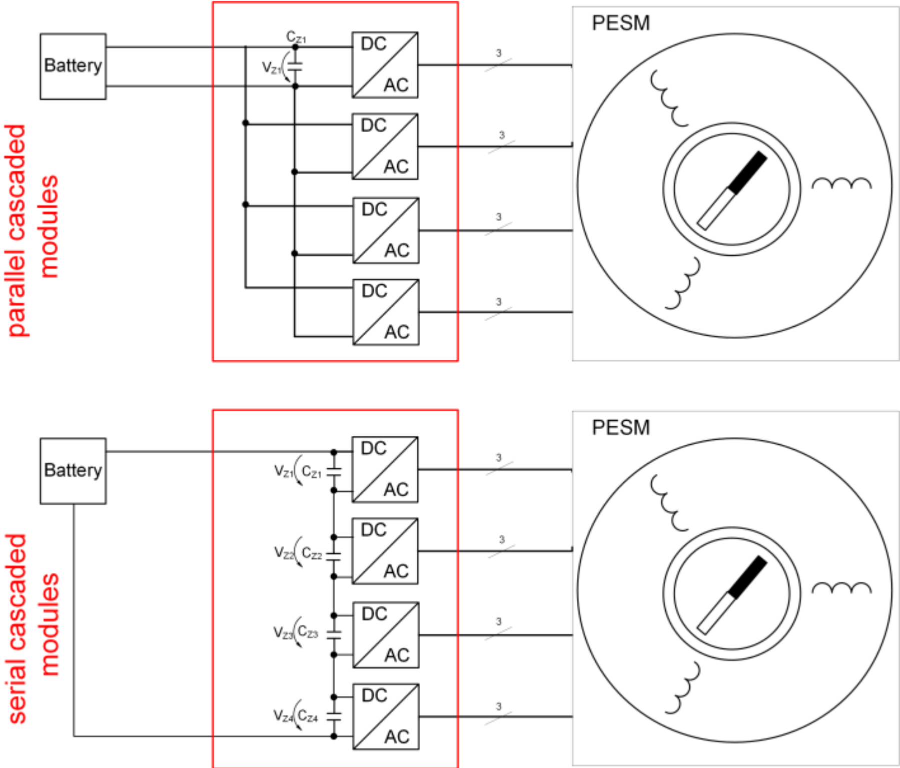

Fig. 2 Parallel cascaded (top) and serial cascaded (bottom) system configuration [7].

The parallel cascaded system is the reference for the following investigation. The results are based on Ref. [7] and summarised in Table 1. The efficiency of classical and cascaded systems are similar under partial load conditions. Due to the high current (500 A @ 25 kW, 48 V) under nominal load conditions the distributed systems (serial and parallel cascaded) outperform the efficiency of the classical system.

This behaviour can be explained by reduced ohmic losses ($P_V = I^2 \cdot R$) in the cascaded systems—distributed

Table 1 25 kW motor inverter topology comparison.

	Classical system	Serial cascaded system	Parallel cascaded system
Battery voltage [V]	48	200	50
Global efficiency [%]	96 %[1)] / 91 %[2)]	97,5 %[1)] / 95 %[2)]	97,5 %[1)] / 94 %[2)]
Gate-driver efforts (number; galvanic isolation)	++	--	-
Control efforts	+	-	-
Safety (low system voltage)	++	-	++
Losses on battery DC link	--	++	--
DC-link capacitor current stress (control pulse pattern optimisation)	-	-	++
DC-link capacitor volume	-	-	++

[1)] efficiency @ partial load (1,000 min^{-1}/30 Nm); [2)] efficiency @ rated load (1,000 min^{-1}/80 Nm).
(++ very good; + good; - bad; -- poor) [7].

current leads to reduced losses. The differences between a parallel cascaded system and a serial cascaded system are marginal, the single power converters in both topologies are identical only the battery supply network is different. The serial cascaded topology has a slight advantage compared to the parallel approach because of lower currents in the battery network and in the DC link to the converter. Both systems require some control efforts for balancing (current in parallel topology, voltage in serial topology). In summary, the parallel cascaded topology offers best performance in high-current systems with the additional advantages of redundancy and battery/bulk capacitor ripple reduction. The next step in the design process is the dimensioning of the active, passive components and the selection of the PCB technology.

2.2 Comparison in PCB Technology

This chapter gives an overview on different PCB technologies for high-current transmission (up to 500 A) and optimal thermal spreading on the PCB. The investigated technologies are: “thick copper”, “Wirelaid”, “Eisberg” and copper inlay technology. Due to cost reduction, easy manufacturing and higher system integration there is a trend of combining high-current structures with fine structures for the gate-driver, sensors and control-circuits in a single board solution e.g. in motor inverters.

A comparison of different PCB technologies in respect of high-current transmission, realisation of fine structures, thermal management and relative costs is summarised in Fig. 3 (based on Ref. [8]). The largest green area marks the system with the best performance regarding high current transmission, good thermal management, good fine structure ability and moderate costs. The cost aspect is only estimated—actual there a no mass production for this topologies established.

The best performance technology is the “Eisberg” technology. This method is based on bottom side copper etching with the advantage of a flat PCB surface. Fine structures as well as high-current and heat transfer areas can be realized by bottom side etching of a 400 µm base copper foil. Costs for this technology are moderate.

The easiest way of developing a high-current PCB is the “thick copper” technology. This method is based on top side copper etching. The thermal design and heat conduction trough the PCB or between the layers in the “thick copper” technology is challenging as a lot of thermal vias are required (see chapter 0). A disadvantage of “thick copper” technology is that fine structures only down to a track width of 250 µm can be realised. “Wirelaid” has a good fine structure ability,

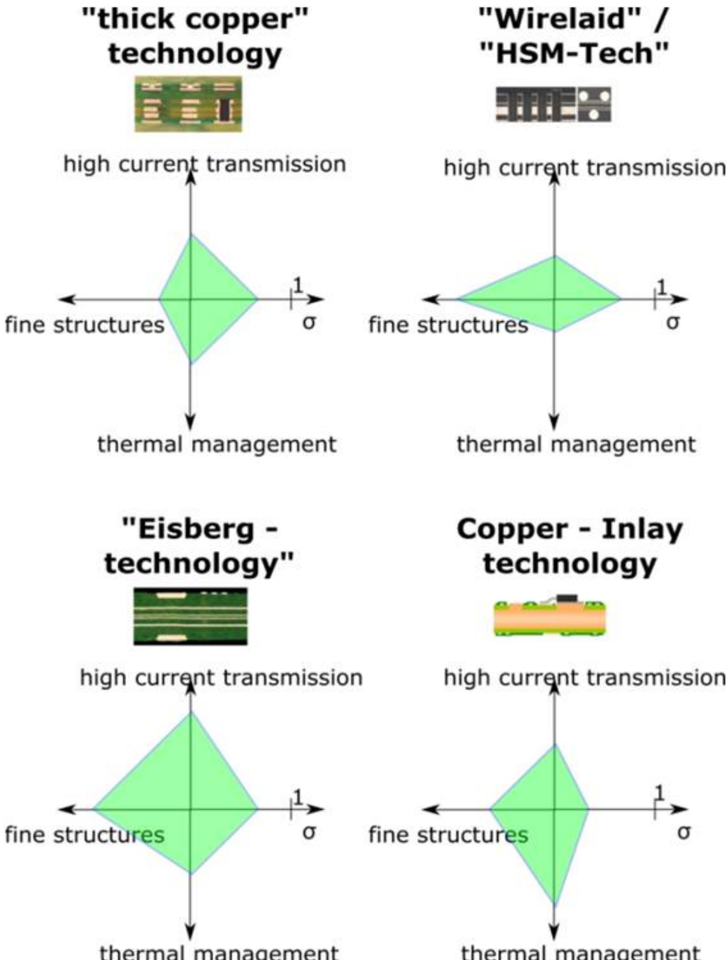

Fig. 3 Overview of different PCB technologies and their characteristics (σ ≙ relative costs = "costs of standard FR4 solution with 35 µm copper" to "costs of the considered technology") [8].

thermal management and current transmission is not excellent. Copper inlay technology is suitable for good thermal management and a good fine structure ability at high costs.

The technologies "thick copper", "Wirelaid" and "Eisberg" need vias for the thermal management. This challenge is investigated in chapter 0.

2.3 Current Measurement in High-Current Systems Inverter Systems

Current measurement is a special topic in high-current systems—high accuracy and low losses are required. In motor inverter applications AC current measurement is based on shunt resistor, transformer or the Rogowski principle. DC current measurement depends on conductive methods like shunt resistors or field measurement methods like hall sensors, integrated hall sensors and magneto-resistive sensors (see Table 2 and Ref. [8]). The shunt resistor can be used for measuring the phase current in two inverter phases. The third phase current is calculated, so two resistors are needed in the inverter. An advanced method is the measurement of the DC link current by a resistor and the estimation of the phase current in the controller. The resistor measurement is popular due to low cost, large measurement bandwidth (limited by the signal processing) and the insusceptibility against electric and magnetic fields. The drawback of the resistor solution is the power loss. The described 25 kW, 48 V integrated motor inverter (reference system—see paragraph 0) was equipped with integrated hall sensor Allegro ACS758 [1] and the hall

Table 1 Overview on current measurement concepts in motor inverter applications (+ good; - bad); picture source: Refs. [1-4].

Sensor principles	Figure	I_{MAX} [A]	Accuracy [%]	Susceptibility magnetic field	Susceptibility electric field	Bandwidth [kHz]
Integrated hall sensor	Sensed Current Source: [1]	< 200	+/- 2	- (shield required)	+ (integrated shield)	120
Hall sensor	B I Source: [2]	< 1000	+/- 5	- (shield required)	- (shield required)	100
Shunt resistor	Source: [3]	< 1000	+/- 0,5	+	+	500 (due to signal processing)
Magneto-resistive sensor	Source: [4]	< 150	+/- 1.5	- (shield required)	- (shield required)	400

sensor Melexis MLX91205 for phase current measurement as well as resistive DC link current measurement (Fig. 4) for comparison. The hall sensor Melexis MLX91205 [2] is very susceptible to interferences with magnetic fields, so this solution is inappropriate for a motor integrated inverter.

The Allegro ACS758 [1] needs also external shielding to withstand the strong magnetic field of the 25 kW synchronous machine. The preferred solution for current measurement considering costs, accuracy, required design space, installation efforts and insusceptibility against electric/magnetic fields is the DC link current measurement by resistor. The solution needs a resistor in the inverter DC link path combined with mathematical algorithms in the controller to assemble the motor phase current by DC link current sections and inverter state. This solution offers moderate values with low hardware efforts—accuracy is dependent on the current measuring range.

2.4 PCB Layout under Thermal Limits—Respect the Cooling Conditions

The current load capacity in many PCB layouts was estimated by the standards IPC-2221 and DIN IEC 326.

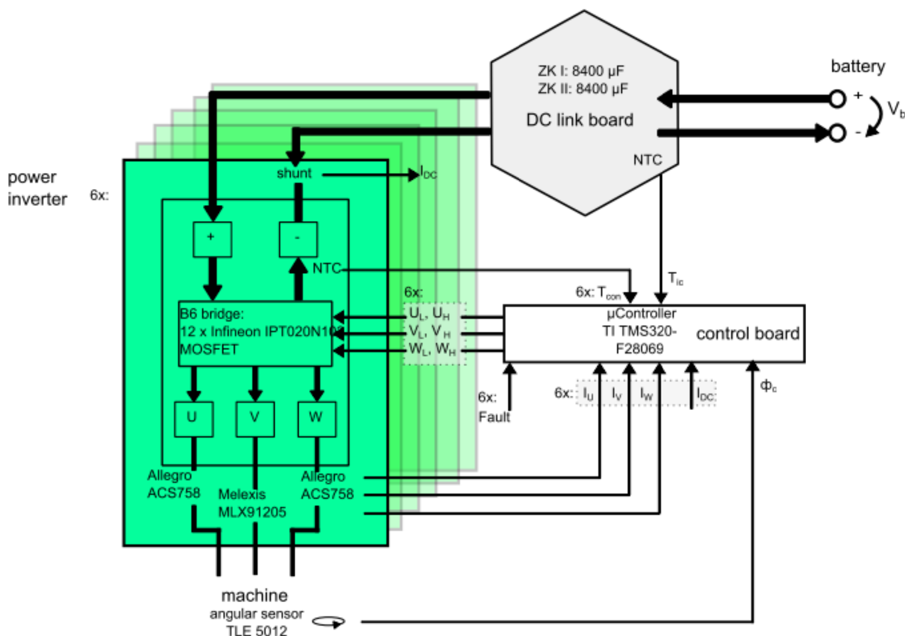

Fig. 4 Principle of the 25 kW, 48 V integrated motor inverter (reference system—see paragraph 0) [8].

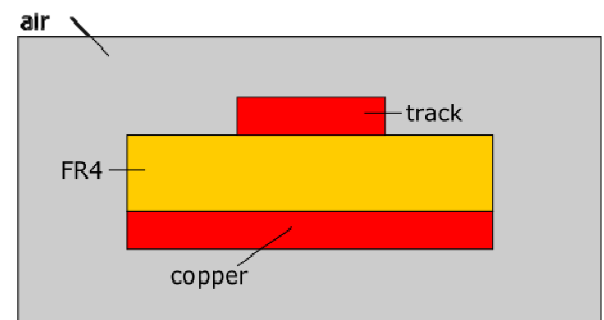

Fig. 5 PCB layout setup used in IPC-2221 and DIN IEC 326 standards—passive PCB cooling by convection.

Fig. 6 Investigated PCB layout setup for high-current systems (thermal conductivity: FR4 0.3 W/mK; solder mask0.7 W/mK; copper 401 W/mK)—active PCB cooling.

They form a very conservative approach since these standards and other contributions [5] base only on thermal convection and radiation. The standard setup is shown in Fig. 5. The track is placed on a plate (e.g. FR4) with an optional copper layer on the backside cooled by air convection and radiation.

For challenging system requirements like those in the high-current systems the standard PCB layout approach need to be rethought. The copper thickness and track width should be adapted to the thermal requirements, the used cooling systems and the PCB manufacturing approach.

The new approach considers the cooling conditions of the PCB. The approach to investigate the high-current systems (Fig. 6) is done by the software “Ansys Workbench 16.2” with the analysis system “thermal electric”, “DC current” and the solver “mechanical”. The simulation of the investigated high-current PCB was done with a constant backside temperature T_{ref} of the PCB (see Fig. 6). This approach gives the freedom in the cooling system. The results can be used for different systems.

2.4.1 Maximise the PCB Utilisation—Fathom the Limits

The following simulation results are done for the configuration shown in Fig. 6 with a varying copper thickness of 35 µm, 70 µm and 105 µm at varied track width.

$$I_{track_standard}[A] = K \cdot h^{0,5}[mm] \cdot b^{0,64}[mm] \cdot \Delta T^{0,5}[K] \quad (1)$$

Eq. (1): PCB current carrying capability according to the standard IPC-2221/ DIN IEC 326 (K = 3.3 @ 2

layer PCB; K = 3.6 @ 4 layer PCB; b= track width; h = track thickness; ΔT = temperature rise) [6].

The results for estimation the current carrying capability at different temperature rise are shown in Fig. 7-9. More concrete are the results in Tables 3-5, here the simulation results for the new cooled PCB approach and the conventional approach are compared. The current carrying capability for the conventional approach can be estimated with Eq. (1) [6]. The results for a PCB with 35 μm copper thickness, different track width for 20 K temperature rise are summarised in Table 3.

The results are very clear, the conventional approach is very conservative and the utilisation of the PCB is insufficient. Due to the direct cooling of PCB the current carrying capability is 5 to 9 times higher than estimated with the conventional approach. The results for 70 μm (Table 4) and 105 μm (Table 5) copper thickness are similar. The analysis of a pure copper track is one part. For a PCB design the investigation of

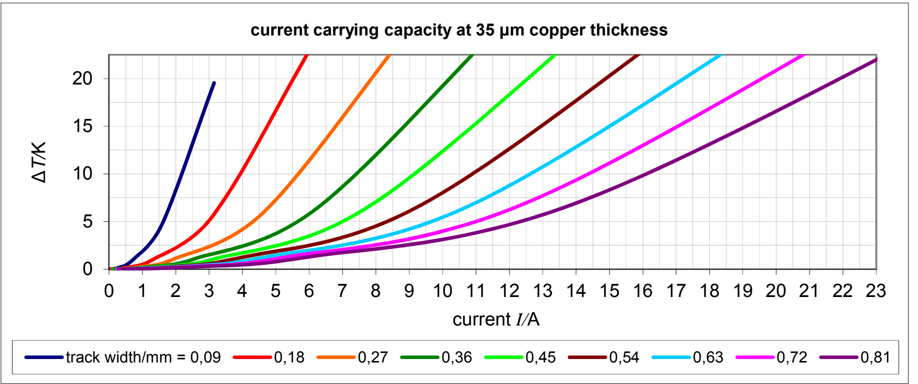

Fig. 7 Determined current carrying capability of different copper tracks @ 35 μm copper thickness.

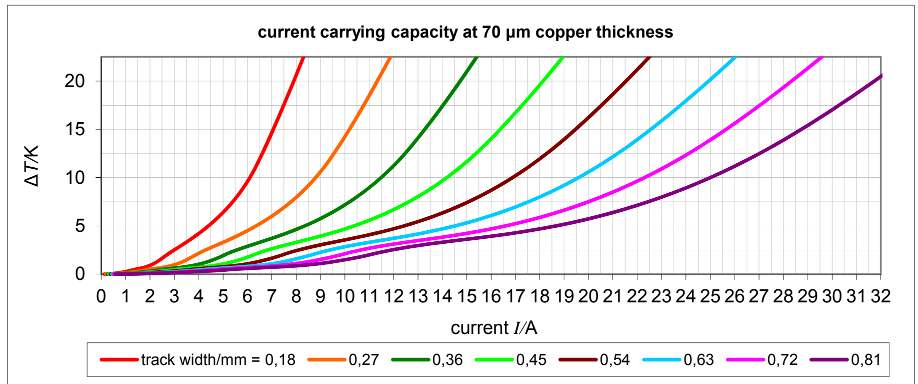

Fig. 8 Determined current carrying capability of different copper tracks @ 70 μm copper thickness.

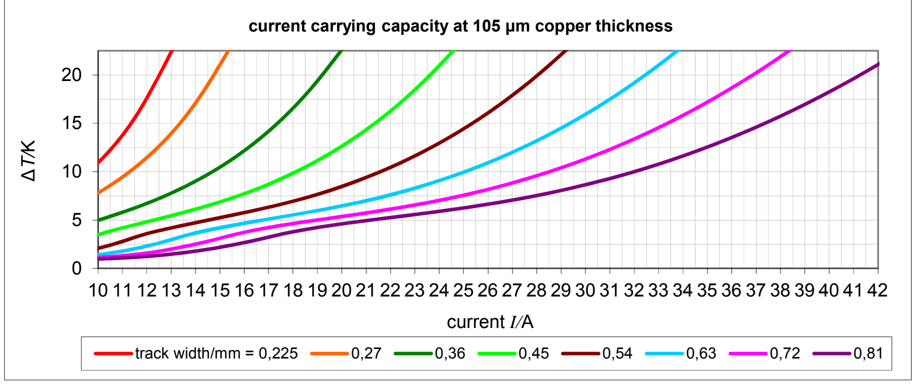

Fig. 9 Determined current carrying capability of different copper tracks @ 105 μm copper thickness.

Table 2 Determined current carrying capability of different copper tracks @ 35 μm copper thickness; comparison between new approach and standard approach.

track width [μm]	I_track_new @Δ*T*=20 K	I_track_standard @Δ*T*=20 K	I_track_new/ I_track_standard
90	3,25 A	0,59 A	550%
180	5,50 A	0,92 A	597%
270	7,80 A	1,19 A	653%
360	10,20 A	1,44 A	710%
450	12,50 A	1,66 A	755%
540	14,80 A	1,86 A	795%
630	17,25 A	2,05 A	840%
720	19,50 A	2,24 A	872%
810	22,00 A	2,41 A	912%

Table 4 Determined current carrying capability of different copper tracks @ 70 μm copper thickness; comparison between new approach and standard approach.

track width [μm]	I_track_new @Δ*T*=20 K	I_track_standard @Δ*T*=20 K	I_track_new/ I_track_standard
180	8,00 A	1,30 A	614%
270	11,40 A	1,69 A	675%
360	14,75 A	2,03 A	726%
450	18,20 A	2,34 A	777%
540	21,70 A	2,63 A	824%
630	25,00 A	2,91 A	861%
720	28,40 A	3,16 A	898%
810	31,75 A	3,41 A	931%

Table 5 Determined current carrying capability of different copper tracks @ 105 μm copper thickness; comparison between new approach and standard approach.

track width [μm]	I_track_new @Δ*T*=20 K	I_track_standard @Δ*T*=20 K	I_track_new/ I_track_standard
225	12,50 A	1,84 A	679%
270	14,75 A	2,07 A	713%
360	19,20 A	2,49 A	772%
450	23,60 A	2,87 A	823%
540	28,00 A	3,22 A	869%
630	32,40 A	3,56 A	911%
720	36,80 A	3,88 A	950%
810	41,20 A	4,18 A	986%

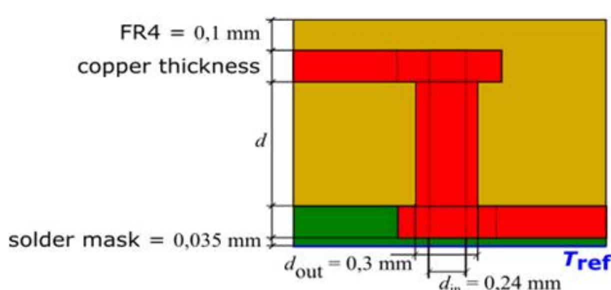

Fig. 10 Investigated PCB layout setup for high-current systems—two layers connected by thermal via—copper cross section constant @ different layer distances.

a copper track across different layers is necessary (see Fig. 10). The cross section of copper track and via was selected identically. The investigation was also done by software "Ansys Workbench 16.2", the results are shown in Fig. 11 and summarised in Table 6.

The current carrying capability of a multi-layer system is reduced by about 30% compared to a high-current single layer system. The thermal vias are the bottleneck for the current. Nevertheless the cooled

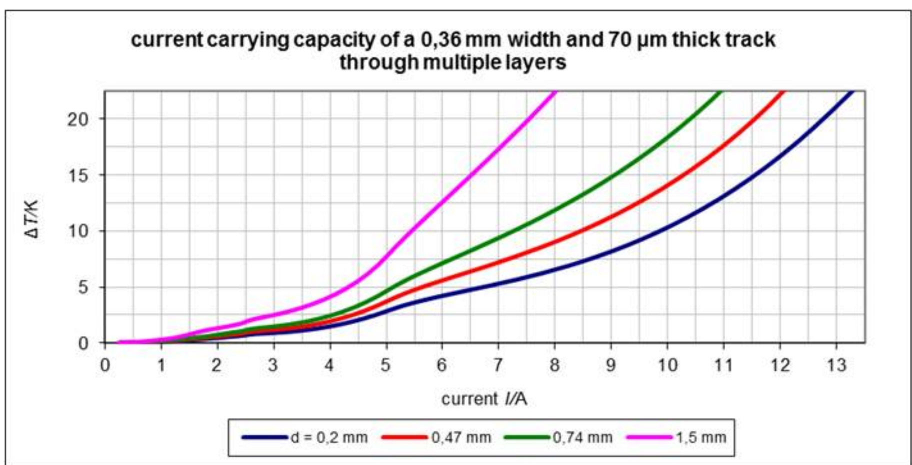

Fig. 11 Determined current carrying capability of a copper track with 0.36 mm width and 70 µm thickness @ different layer distances (d).

Table 3 Determined current carrying capability of a copper track with 0.36 mm width and 70 µm thickness @ different layer distances (d)—comparison between single track approach (I_track_new—Table 4) and copper track across different layers (I_track_via— Fig. 11).

layer distance d [µm]	I_track_via @Δ*T*=20 K	I_track_new @Δ*T*=20 K, 360 µm track width, 70µm track thickness	I_track_standard @Δ*T*=20 K, 360 µm track width, 70µm track thickness	I_track_via/ I_track_standard
200	12,80 A	14,75 A	2,03 A	631%
470	11,50 A	14,75 A	2,03 A	567%
740	10,40 A	14,75 A	2,03 A	512%
1500	7,50 A	14,75 A	2,03 A	369%

multi-layer system with a constant backside temperature T_{ref} can carry about five times higher current than estimated with the conventional approach (see Fig. 5). These results are only a detail of the complete investigation. They are done for different layer- and material configurations also include different semiconductor packages, via dimensions and amount. These results were shown in future publications.

2.5 Optimisation of the DC Link

The design of the commutation cell, the connection between the DC link capacitor and semiconductor is very important. This connection needs to be very low inductive to avoid large voltage overshoot at the semiconductors and to realise fast switching. This paragraph deals with the question of the DC link cap setup—pure electrolytic capacitors versus electrolytic capacitors and ceramic capacitors together. Furthermore different bulk capacitor interconnection schemes are investigated.

2.5.1 Investigation and Optimisation of DC Link Capacitor Interconnection

The bulk capacitor in high-current systems is stressed with high-current pulses, the interconnection needs to be very low inductive (L_{C1}, L_{C2} in Fig. 12) to avoid voltage overshoot in the power switch network. Due to design space requirements the electrolytic bulk capacitors (C_{EC}) cannot be connected directly to the semiconductor switches. The solution is the placing of some extra ceramic capacitors C_{CC} and the adjustment of the current sharing—ceramic should handle the pulses. The main energy should come from the electrolytic capacitor.

The real situation is different. The current sharing between both capacitor systems is dependent on the resistive and inductive conditions. Normally the ceramic capacitors are very close to the switching cell, hence they have to carry almost the complete system current, which they usually are not able to withstand.

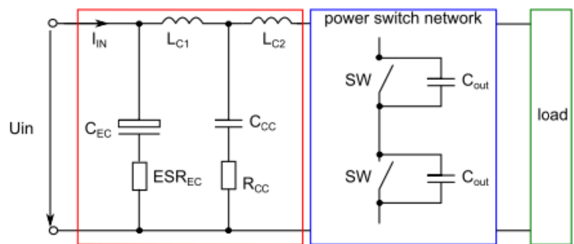

Fig. 12 Equivalent circuit of an inverter system to investigate the bulk capacitor current sharing (U_{IN}= 48 V; I_{Phase} = 200 A; C_{EC} = 2 mF; C_{CC} = 14 μF; L_{C1} = 10 nH; L_{C2} = 10 pH).

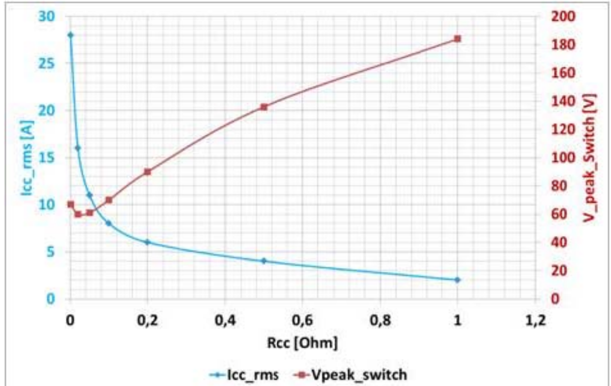

Fig. 13 Results of the serial resistor R_{CC} optimisation in a combined DC link—influence to ceramic capacitor current stress (I_{CC}) and semiconductor peak voltage (V_{peak_switch}).

The ceramic capacitors would be destroyed. A solution for effective current load sharing and switch peak voltage limitation is the introduction of a serial resistor R_{CC} in the ceramic capacitor path. The influence of R_{CC} to the ceramic capacitor current stress (I_{CC}) and semiconductor peak voltage (V_{peak_switch}) is shown in Fig. 13. A resistor R_{CC} of 20 mΩ leads to a minimum voltage stress of 60 V_{peak} at the semiconductor switches and to a ceramic capacitor current stress of 16 A (14 caps in parallel)—valid for the system in Fig. 12. Concluded, a shared DC link capacitor with balanced ceramic capacitors is a good possibility for high-current system design.

2.5.2 Use of a Pure Ceramic DC Link

A conventional DC link consists of electrolytic capacitors with the advantages of high energy density and low price. The disadvantages like limited lifetime and large space requirements can be overcome by use of a pure ceramic DC link capacitor. This paragraph shows the investigation results under the following conditions (for capacitor): total required capacity > 6,000 μF; electric strength 100 V; bias voltage 52 V; dielectric medium X7R due to thermal requirements; area per PCB side 9,385 mm². The design problems are: the required dielectric material X7R limits the selection of capacitors, the capacity of ceramic capacitors depends on the bias voltage—the bias voltage reduces the usable capacity. The energy density of different DC link capacitor solutions is compared in Fig. 15. The ceramic capacitors (MLCC) in package 1206 offer the best volume energy density, even higher than an electrolytic capacitor. For system design the area energy density is crucial—the comparison related to the ground area shown in Fig. 16. The electrolytic capacitor offers best energy density per ground area.

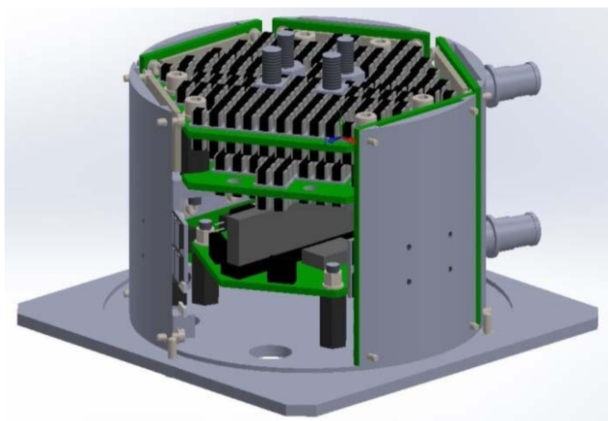

Fig. 14 System model of a 48 V-25 kW motor inverter with pure ceramic DC link capacitor.

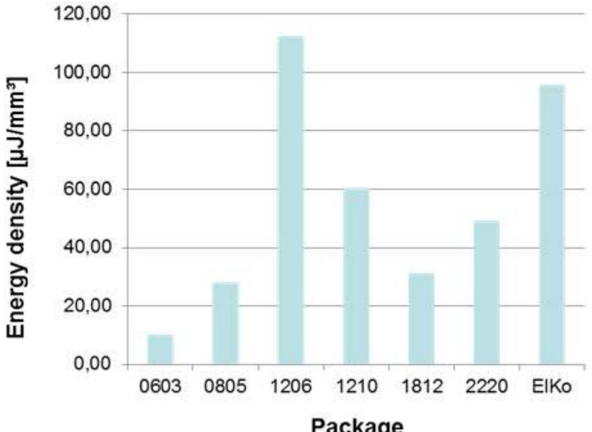

Fig. 15 Energy density of different DC link capacitors—related to the device volume (MLCC vs. electrolytic capacitors).

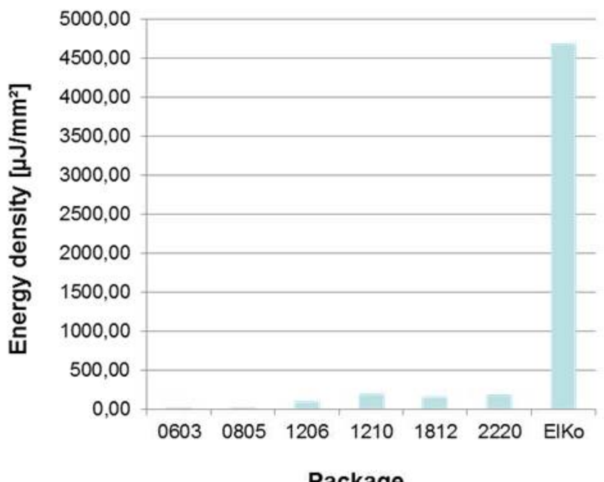

Fig. 16 Energy density of different DC link capacitors—related to the device ground area (MLCC vs. electrolytic capacitors).

Fig. 17 Cost comparison of different DC link capacitor solutions (MLCC vs. electrolytic capacitors).

The comparison of costs for the DC link (see Fig. 17) shows also a clear result, the electrolytic capacitor solution with an estimated price of 48€ for 15.6 mF capacity is 24 times less expensive than the MLCC (package 2220) DC link with 1,150€ costs for 5.01 mF capacity.

Concluded, a ceramic (MLCC) DC link is only a solution for special application with extreme lifetime and volume requirements. Electrolytic capacitors are the best solution for DC link in conventional applications.

2.5.3 Considerations on Low Inductance DC Link

The design of the commutation cell is very important for the switching behaviour and efficiency of a low-voltage high-current inverter. This paragraph deals with the optimisation of the inductance in the interconnection between DC link capacitor and semiconductor switches. The optimisation was done by simulation with the tool "Ansys Electromagnetics, Maxwell 3D", solution type: Magnetic—Eddy Current with analysing setup: frequency sweep in the range from 20 kHz to 10 MHz. The wide frequency range was used to consider also the behaviour of the inductance at high frequency of several MHz, like applied during switch commutation. The different configurations of track setup for DC link connection are shown in Fig. 18 to Fig. 27. The results of the simulations are concluded in Fig. 28 and Fig. 29—please note the values are associated to the named track dimensions. Shielding of the tracks was tested in the type 2 (Fig. 19) and type 3 (Fig. 20) configuration—the shielding shows a positive effect for reduction DC link inductance compared to type 1 (Fig. 18). A stacked setup type 4 (Fig. 21) is better than a side by side setup type 1 (Fig. 18).

An interlace wire system like type 5, 6, 7 (Fig. 22 to Fig. 24) (about 60 nH per meter track) brings advantages

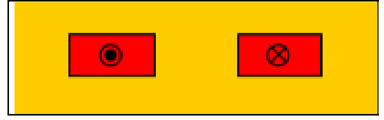

Fig. 18 Type 1—2 tracks (105 µm track height, 5 mm track width, 4 mm track distance) in 1 layer.

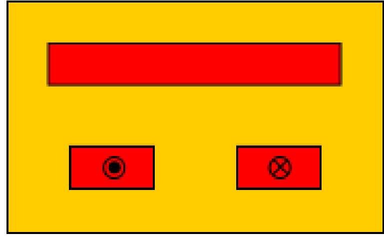

Fig. 19 Type 2—2 tracks (105 µm track height, 5 mm track width, 4 mm track distance) in 1 layer + 105 µm shielding layer@ GND (0.5 mm layer distance).

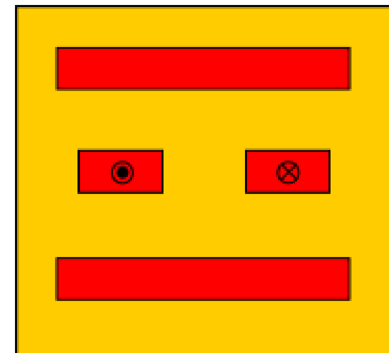

Fig. 20 Type 3—2 tracks (105 µm track height, 5 mm track width, 4 mm track distance) in 1 layer + two 105 µm shielding layers @ GND (0.5 mm layer distance).

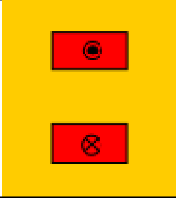

Fig. 21 Type 4—2 tracks (105 μm track height, 5 mm track width) in 2 layers (0.5 mm layer distance).

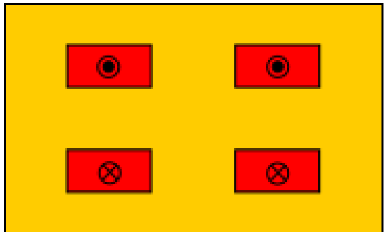

Fig. 22 Type 5—4 tracks(105 μm track height, 5 mm track width, 4 mm track distance) in 2 layers (0.5 mm layer distance).

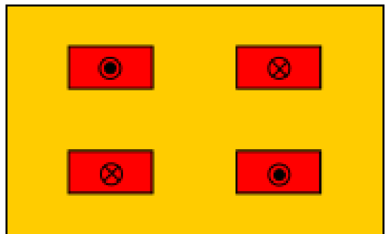

Fig. 23 Type 6—4 tracks (105 μm track height, 5 mm track width, 4 mm track distance) in 2 layers (0.5 mm layer distance).

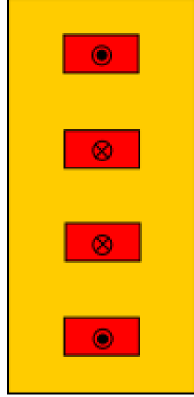

Fig. 24 Type 7—4 tracks (105 μm track height, 5 mm track width) in 4 layers (0.5 mm layer distance).

regarding low DC link inductance.

The lowest inductance can be achieved with a configuration like type 8 (Fig. 25), with an inductance of about 40 nH per meter track length (Fig. 29)—e.g. 10 cm long configuration like type 8 on a PCB has 4 nH inductance. For lowering the inductance both tracks should have large track width. Crossed tracks like type 10 (Fig. 27) have a large inductance, similar with the side by side setup type 1 (Fig. 18) due to a larger stretched area between the tracks.

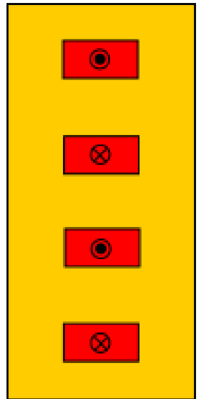

Fig. 25 Type 8—4 tracks (105 μm track height, 5 mm track width) in 4 layers (0.5 mm layer distance).

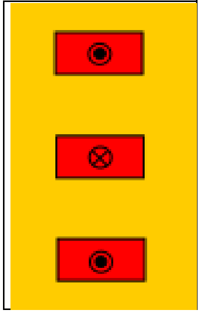

Fig. 26 Type 9—3 tracks (105 μm track height, 5 mm track width) in 3 layers (0.5 mm layer distance).

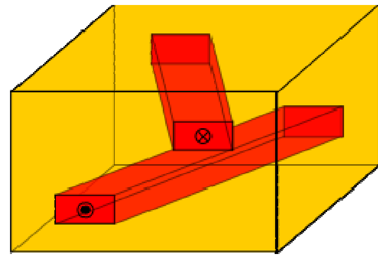

Fig. 27 Type 10—2 crossed tracks (105 μm track height, 5 mm track width, 4 mm track distanceat the end of track) in 2 layers (0.5 mm layer distance).

The leakage inductance of the DC link interconnection corresponds directly to the voltage stress and the losses in the semiconductor switches (see Fig. 30). For an adequate semiconductor voltage stress the stray inductance in the DC link should be less than 10 nH. This means by using the configuration type 8 (Fig. 25) with 105 μm track height, 5 mm track width

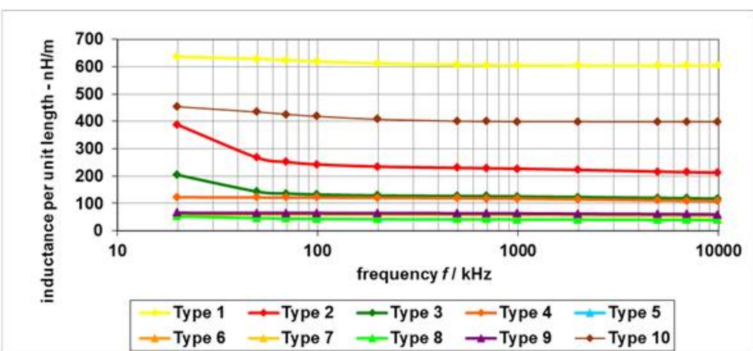

Fig. 28 Inductance over frequency of the different track configurations per meter track length @ 105 µm track height, 5 mm track width, 4 mm track distance.

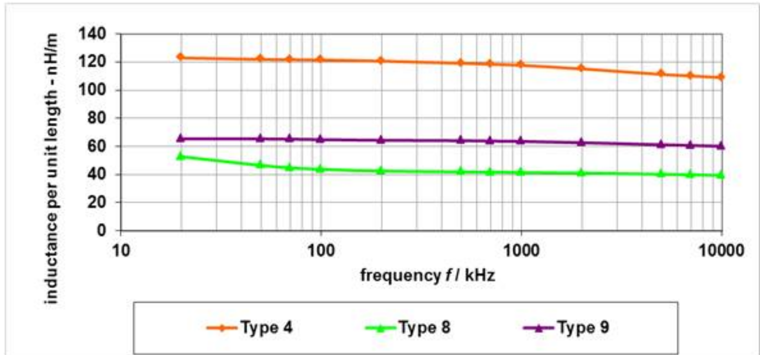

Fig. 29 Inductance over frequency of selected low inductance track configurations per meter track length @ 105 µm track height, 5 mm track width, 4 mm track distance.

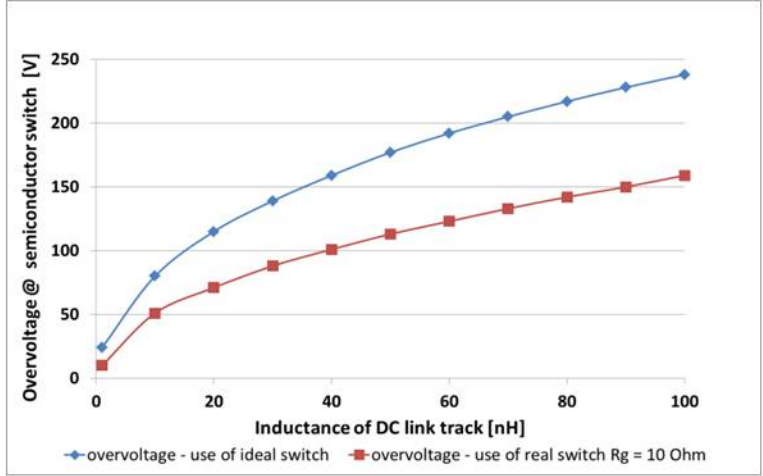

Fig. 30 Overvoltage V_{DS_peak} @ MOSFET switch in buck configuration (V_{DC_Link} = 48 V; I_{OUT} = 100 A) at varied inductance of the DC link interconnection.

in 4 layers with 0.5 mm layer distance a maximum track length of 25 cm. This is the main challenge in low-voltage systems.

3. Conclusion

This article provides an overview on challenges in low-voltage high-current systems used in automotive applications. The selection of the inverter topology for high current systems was investigated—a serial cascaded system is best due to global efficiency, a parallel cascaded system is best due to system safety. By implementation the topology in a PCB different

techniques are possible—the best performance technology regarding high current transmission, good thermal management, good fine structure ability and moderate costs is the “Eisberg” technology. Fine structures as well as high-current and heat transfer areas can be realized by bottom side etching of a 400 μm base copper foil. The combination of high-current structures with fine structures for the gate-driver, control-circuits and sensors in a single board solution is an actual challenge.

The different sensors for current measurement are investigated—the resistive method by measuring DC link current and assemble the motor phase current by DC link current sections and inverter state in the controller is favoured due to losses and design space. This solution offers accurate values with low hardware efforts.

The design space is a major topic in automotive applications, it can be influenced also by the PCB utilisation—a new design approach for simulation the current carrying capability of a PCB shows a about three times higher current carrying capability compared to the standards IPC-2221 and DIN IEC 326 by considering the real cooling conditions of the PCB. This means the current carrying capability of a high current PCB needs to be investigated to reach good system utilisation. Improvement of utilisation is also possible by optimised DC link interconnection—a interleaved track configuration reduces track inductance more than 90% compared to a side by side track setup. Low DC link inductance leads to low inverter voltage stress and high efficiency. In future market for low-voltage high-current systems in automotive area will increase, so the system design topic becomes more important.

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