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# Problems and Properties of a Current Amplifier When Realized in Ultra Deep Sub-micron Technology

Simeon Kostadinov[1], Ivan Uzunov[2] and Dobromir Gaydazhiev[3]

*1. Smartcom Bulgaria AD, Department of Microelectronics, 36 Dragan Tzankov blvd., Sofia 1040, Bulgaria*

*2. SmartLab AD, BIC IZOT, Build. 1, 133 Tzarigr. Shosse blvd., Sofia 1784, Bulgaria*

*3. Smartcom Bulgaria AD, Department of Microelectronics, 36 Dragan Tzankov blvd., Sofia1040, Bulgaria*

**Abstract:** The paper considers the problems related to short-channel effects in a current amplifier, when realized in ultra-deep sub-micron technology. A short description of the circuit and a limitation concerning its basic parameters is given at the beginning. Several steps, allowing an approximate design of the circuit, are outlined. They are applied for design of three versions of the amplifier, each of them is realized with FETs having different channel length: 90 nm, 45 nm and 30 nm. Their basic properties are simulated and discussed, demonstrating the major benefit of the shortening of the channel length—extension of the frequency bandwidth. The problems arising with the shorter channels length are also considered briefly.

**Key words:** Amplifiers, current mode operation, short-channel effects, MOSFET.

## 1. Introduction

The scaling of the semiconductor devices in modern CMOS technology improves the performance, lowers the price and reduces the power supply of the fabricated circuits [1, 2]. While device downscaling is driven primarily by the benefits it has in digital design, it introduces new effects in transistor behavior, which makes analog design challenging. As channel lengths decrease below 1 μm, second order effects, which were not taken into account for long channel FETs must be accounted for. When short channel effects become significant the traditional analytic approach in analog design is not feasible [3]. This necessitates a modification of the existing analytic design methodologies and employment of new techniques.

Shrinking the gate length is accompanied by decrease in power supply voltage, which is a major issue in analog design. However threshold voltage does not scale as much as the supply voltage, and transistors are biased at lower voltages, which results in worse transistor properties [1, 4].

**Corresponding author:** IvanUzunov, M.Sc., Ph.D., expert, research fields: circuit theory, filters, analog IC.

Current mode operation overcomes some of the problems with downscaling because it requires lower supply voltage compared to its voltage mode counterparts [4, 5]. It also has some other advantages —at low power supply voltage they allow wider signal dynamic range, wider frequency bandwidth, better linearity. For these reasons, current mode designs become very popular in many high performance analog and mixed signal applications — RF front ends, data converters, oscilatiors, etc.

The legacy design methodology applicable for long channel devices uses theoretical circuit analysis based on expressions taking into account only first order effects. In contrast, designing an amplifier in sub-micron technology must include the higher order effects, rendering a purely analytical approach no longer viable, since it leads to significant inaccuracies mainly related to the specific short channel effects—drain induced barrier lowering, channel length modulation, velocity saturation [1, 3, 4]. Even some technology specific parameters, e.g., $\mu C_{ox}$, are not constant anymore and depend on transistor geometry.

A method for design of a basic current amplifier, when short channel effects are significant is proposed in Ref. [6]. For the cases when short channel effects are moderate the design procedure gives very good matching between specification and simulation results. Further reduction of device sizes causes more and more deviation from the basic theory. The goal of this paper is investigation of these effects when the sizes approach the technology defined limits. A basic current amplifier is designed with different FET devices having different channel lengths. The used process is 32 nm bulk CMOS technology, developed by IBM for SRAM, logic and mixed-signal applications [7]. Three versions of the amplifier are considered: (1) realized with hpar FETs with gate length of 90 nm; (2) realized with slvt FETs with gate length of 45nm; and (3) realized with slvt FETs with gate length of 30 nm (the minimum allowed drawn gate length for thin oxide in the used 32 nm technology). The abbreviations hpar and slvt are for different types of MOS transistors in the Process Design Kit [7].

## 2. The Circuit: Operation and Relations between Its Basic Parameters

The circuit of a basic current amplifier is shown in Fig. 1 and its operation is based on several connected current mirrors [5]. In quiescent point, the reference current $I_b$ is copied through current mirrors $M_{10}$-$M_9$ and $M_2$-$M_1$ as a current through $M_1$. The same current is copied in $M_3$ trough $M_{12}$-$M_{11}$ and $M_4$-$M_3$. Current mirrors $M_5$-$M_6$ and $M_7$-$M_8$ copy the identical currents through $M_1$ and $M_3$ as identical currents through $M_6$ and $M_8$ and the output current $I_o$ is zero. The input current $I_i$ disbalances the currents in the upper ($M_1$ and $M_5$) and the lower ($M_3$ and $M_7$) parts of the input branch. A proportional disbalance appears in the output branch and the difference between $M_6$ and $M_8$ drain currents flows through $R_L$ as output current $I_o$. The formulas for the basic amplifier parameters are in Refs. [8-10]:

$$A_i = \frac{W_6/L_6}{W_5/L_5} = \frac{W_8/L_8}{W_7/L_7} \quad (1)$$

$$R_i = \frac{1}{g_{m1}+g_{mb1}+g_{m3}+g_{mb3}} \quad (2)$$

$$R_o = \frac{1}{g_{ds6}+g_{ds8}} \quad (3)$$

Where, $A_i$ is the current gain (output is short circuited), $R_i$ is the input resistance, $R_o$ is the output resistance, $g_m$'s are the transconductances, $g_{mb}$'s are the back-gate transconductances and $g_{ds}$'s are the output conductances of the corresponding FETs. These three parameters are in mutual relation, which can be seen from the following considerations. If assume equal $g_m$'s of $M_1$ and $M_3$ and $g_{mb} \approx 0.1g_m$ then the input resistance can be expressed as:

$$R_i \approx \frac{1}{2.2g_m} \approx \frac{V_{eff1,3}}{4.4I_{D1,3}} \quad (4)$$

Where, $V_{eff1,3}$ and $I_{D1,3}$ are the effective voltage and the DC drain current of $M_1$ and $M_3$. The effective voltages of $M_1$ and $M_3$ could differ slightly, especially in the case of short channels, and then $V_{eff1,3}$ is their average. The formula for the MOSFET output conductance $g_{ds} \approx \lambda I_D$ [2] allows to rewrite the expression for $R_o$ in the following way

$$R_o \approx \frac{1}{(\lambda_6+\lambda_8)I_{D6,8}} \quad (5)$$

assuming equal DC drain currents ($I_{D6,8} = I_{D6} = I_{D8}$). The current gain is equal to the ratio between DC currents in the output and in the input branches ($A_i = I_{D6,8}/I_{D1,3}$) and this relationship, together with Eqs. (4) and (5), gives:

$$\frac{A_i R_o}{R_i} \approx \frac{4.4}{(\lambda_6+\lambda_8)V_{eff1,3}} \quad (6)$$

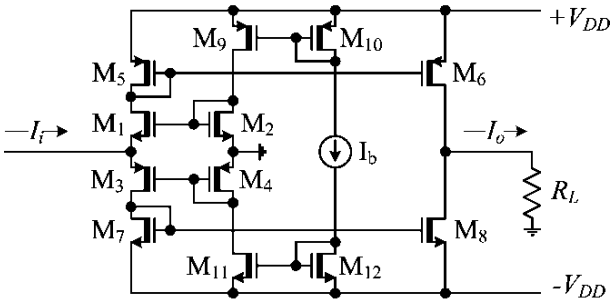


**Fig. 1 The circuit of the current amplifier.**

A decent current amplifier should have high output resistance, low input resistance and current gain greater than 1, i.e. the value of the expressions in Eq. (6) should be very large (ideally infinite). This value is defined by the effective voltage of the input FETs and by the channel-length modulation parameters of the output FETs, which should be as small as possible. However, this condition is in contradiction with other requirements. A small effective voltage limits the frequency bandwidth. Also, it reduces $g_m$ according Eq. (7):

$$g_m = \mu C_{ox} \frac{W}{L} V_{eff} \tag{7}$$

Where, $\mu$ is the carrier mobility, $C_{ox}$ is gate capacitance per unit area, $W$ and $L$ are channel width and length. Consequently it increases $R_i$ as it follows from Eq. (2).

Channel-length modulation parameters are small only for relatively long channels. It increases significantly with shortening of the channel and in deep submicron processes it is not defined at all (see for example Ch. 17 in Ref. [2]). However the limitation about $A_i$, $R_i$ and $R_o$ introduced by the right hand side of Eq. (6) remains, but the expression is more complex and includes more parameters.

## 3. Brief Review of the Design Method

The major problem in the design is the requirement of identical transconductances of $M_1$ and $M_3$ at the same drain currents. This is necessary in order to keep the symmetry in upper and lower halves of the circuit. For long channels $g_m$ is given by Eq. (7) and the drain current is in Refs. [2, 5]:

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{eff}^2 (1 + \lambda V_{DS}) \tag{8}$$

Where, $V_{DS}$ is drain-source voltage of the transistor. The widths of $M_1$ and $M_3$ should be connected with the *n*- and *p*-carriers mobilities by the relationship $W_1/W_3 = \mu_p/\mu_n$ in order to have equal $g_m$'s of these transistors [6]. It follows from Eqs. (7) and (8), but it is valid for long-channel transistors only.

The above mentioned reasons do not allow to implement this relationship for short channel transistors. The design procedure proposed in Ref. [6] uses a graphical and analytical approach for initial design centering and then refining the device dimensions by parametric simulation. The proportionality between $g_m$ and $W$ and between $I_D$ and $W$ allows to introduce a normalizing of the these variables concerning $W$ and the functions $g_{mn}(V_{GS}) = g_m(V_{GS})/W$ and $I_{Dn}(V_{GS}) = I_D(V_{GS})/W$ do not depend on $W$. Short channel violate the above proportionality and there are small variations in the curves representing $g_{mn}(V_{GS})$ and $I_{Dn}(V_{GS})$ at different widths. However these differences are small and can be compensated in the following optimization. Fig. 2 shows corresponding plots received by simulation of 90 nm hpar FETs of the considered technology.

The next design steps are:

(1) The transconductance of the input transistors are defined by the input impedance:

$$g_m = g_{m1} = g_{m3} = \frac{1}{2.2R_i} \tag{9}$$

A normalized value of $g_{m1}$ for NMOS is chosen in the linear region of the curve (Fig. 2(a)). This choice should take into account two other considerations:

(a) The normalized $g_{m1}$ defines $V_{GS}$ and the effective voltage $V_{eff1}$ of $M_1$. A good practice is $V_{eff1}$ to be about 10-15% from the supply voltage $V_{DD}$ in order to guarantee operation in strong inversion and to achieve better frequency bandwidth.

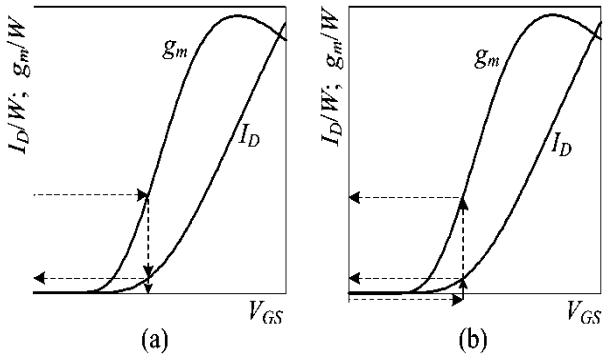


**Fig. 2 Plots of normalized $I_D$ and $g_m$ vs. $V_{GS}$: (a) NMOS; (b) PMOS. The scales for $I_D$ and $g_m$ are different.**

(b) The value of $V_{GS}$ defines also the normalized value of $I_{D1}$ of $M_1$, which should fall in approximately quadratic part of the curve $I_{Dn1}(V_{GS})$(Fig. 2(a)).

(2) The width of $M_1$ can be determined by dividing the desired transconductance, calculated in Eq. (9), by its chosen normalized value. Then the value of the required drain current of $M_1$ is calculated.

(3) The drain currents for $M_1$ and $M_3$ must be the same and equal to the total input branch current — $I_{D1} = I_{D3} = I_D$. Looking at Fig. 2(b) we pick a value $I_{Dn3}$ again in the region where drain current is a quadratic function of $V_{GS}$. This value also defines the $V_{GS}$ and the width of $M_3$.

(4) For the selected value of $I_{Dn3}$ it should be verified that the corresponding $g_{mn}$ is in the linear region in Fig. 2(b). If it is not, another value of $I_{Dn3}$ should be chosen.

(5) These steps do not guarantee the exact matching of $g_{m1}$ and $g_{m3}$ since the transistors are of different types. They could be repeated if the difference is large, however very close matching is not necessary. The received values will be used as initial for the following optimization based on parametric analysis, in which the values of $g_{m1}$ and $g_{m3}$ are equalized at the same drain current.

(6)Transistors $M_5$ and $M_7$ have the same dimensions as $M_3$ and $M_1$ correspondingly. The sizes of transistors $M_6$ and $M_8$ are defined by the required current gain $A_i$ according Eq. (1).

## 4. Problems Arising with Device Downscaling

The described design procedure is applied for design of three versions of the amplifier: (1) with 90 nm hpar FETs; (2) with 45 nm slvt FETs; and (3) with 30 nm slvt FETs. All three versions are supposed to meet the following specifications:

- input impedance $R_i$<500 Ω;
- power supply $V_{DD}$=±1 V;
- current gain $A_i$ equal to 1, i.e. current buffer.

The output impedance is not specified as design parameter, since it can't be arbitrarily chosen, as it follows from the considerations in Section 2.

The design is based on the procedure outlined in the previous section. All transistors are working in strong inversion in saturation and the corresponding DC branch currents are listed in Table 1.

Several problems were faced during the design:

(1) Due to channel length modulation the current mirrors ratios depend strongly on the drain-source voltage. Then the current gain deviates from the ratio of the areas $M_5/M_6$ and $M_7/M_8$ (the theoretical value of the gain). For example, if these transistors have equal areas, the gain for Version 1 is 1.18, for Version 2 it is 1.25, and for Version 3 it is 1.3. An accurate value of current gain can be achieved by varying the channel widths with parametric analysis.

(2) Decreasing the channel length relatively reduces the back-gate transconductance $g_{mb}$ concerning the main transconductance $g_m$. In Ref. [6], $g_{mb}$ is estimated as more than 10% of $g_m$ and its contribution is reflected in Eq. (9) by the factor 2.2. For shorter channels $g_{mb}/g_m$ is less than 5% and this factor should be reduced to 2.1 or even 2.

(3) The threshold voltage $V_{th}$, which is usually considered to be constant, in fact depends on the drain-source voltage $V_{ds}$ due to drain induced barrier lowering (DIBL effect). This is a common short channel effect in FETs. The variation of the threshold voltage is investigated by simulation for the used transistors and the corresponding plots are shown in Fig. 3.

Several effects are observed in Fig. 3. As expected, shorter channels have greater dependence of $V_{th}$ on $V_{DS}$. Transistor type hpar is optimized for analog

**Table 1 DC currents in the amplifier branches.**

| Current in μA through | $I_b$ | $M_5$, $M_1$, $M_3$, $M_7$ | $M_9$, $M_2$, $M_4$, $M_{11}$ | $M_6$, $M_8$ |
|---|---|---|---|---|
| Version 1 | 74 | 72.6 | 73.2 | 98.4 |
| Version 2 | 93 | 79.3 | 85.7 | 121.5 |
| Version 3 | 115 | 97.6 | 105.4 | 186 |

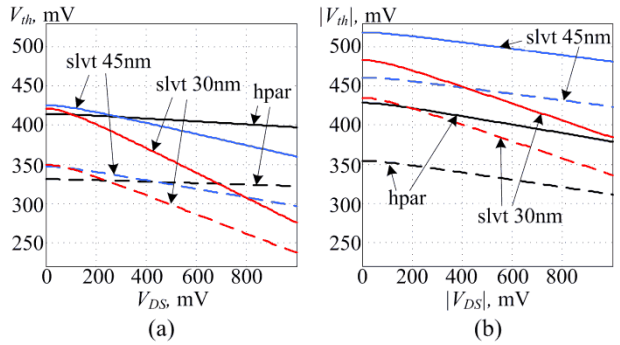


**Fig. 3 Dependence of the threshold voltage from the drain-source voltage for the transistors of interest. Solid lines—with bulk effect, dashed lines—without bulk effects: (a) NMOS; (b) PMOS.**

applications, which results in negligible difference of threshold voltages for PFET and NFET and their deviation with $V_{DS}$. This is not the case for slvt FETs, which are basically intended for use in digital circuits —$V_{th}$ has stronger dependence on $V_{DS}$ and the difference between $V_{th}$ of PFET and NFET is more than 20%. However overcoming the challenges in amplifier design based on slvt FETs proposes some significant benefits—small die area and operation at higher frequencies.

(4) The breakdown voltages for the used transistors are low (1 V) for all three types. On the other hand, threshold voltages are relatively high —up to 0.5 V, while the circuit has four transistors in series in most of the branches. Both circumstances require operating at a total supply voltage, which is more than the limits of the transistors and here ±1 V is used. To guarantee the safe operation it is necessary to check the voltages over transistors at different input current. The limits for the magnitude of the input currents are defined with the following procedure: a DC current source is applied at the input and its current is varied from -3 mA to 3 mA with DC sweep analysis. The plots of the voltages, which exceed the limits, are given in Fig. 4 for amplifiers with hpar and slvt 45 nm. The corresponding plots for slvt 30 nm are very similar to slvt 45 nm and they are not shown. The maximum input current $I_{imax}$ determined from the figure are: 1.2 mA for Version 1 (hpar), and 1 mA for Versions 2 and 3 (slvt).

## 5. Simulations of the Basic Amplifier Parameters

The three versions of the amplifier are compared by several basic parameters: small and large signal current gain, input impedance, and transfer characteristic ($I_o$ vs. $I_i$) and THD. The small signal parameters are shown in Fig. 5. The current gain is different for the three versions for reasons commented above. More interesting are the frequency bandwidths. The corners frequencies are: 12.03 GHz for Version 1, 25.6 GHz for Version 2 and 45.9 GHz for Version 3. For comparison, the same amplifier designed with another type of MOSFETs from the same technology —zgfets with 270 nm minimum gate length [6] has corner frequency of 2.3 GHz. The benefit of using short channel transistors is obvious. The input impedance is close to the designed and it keeps its value up to few GHz.

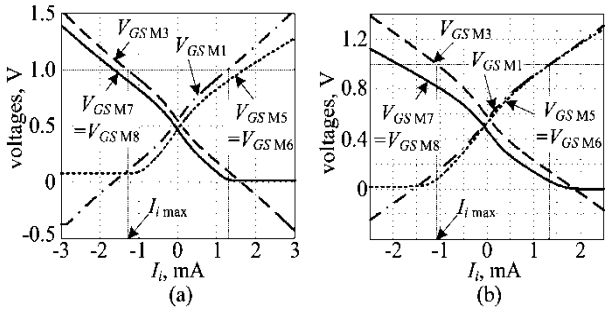


**Fig. 4 Gate-source voltages, which exceed the safe operation range: (a) amplifier with hpar FETs; (b) amplifier with slvt 45 nm FETs.**

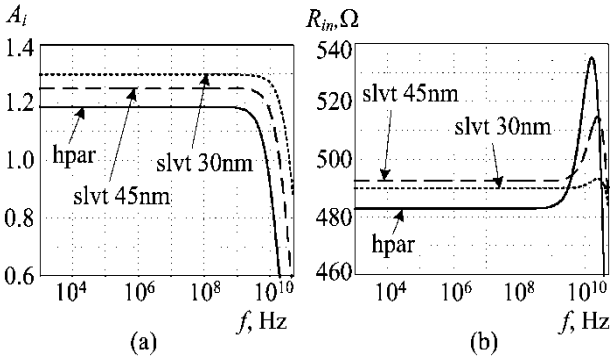


**Fig. 5 Small signal characteristics of the designed amplifiers: (a) current gain; (b) input impedance.**

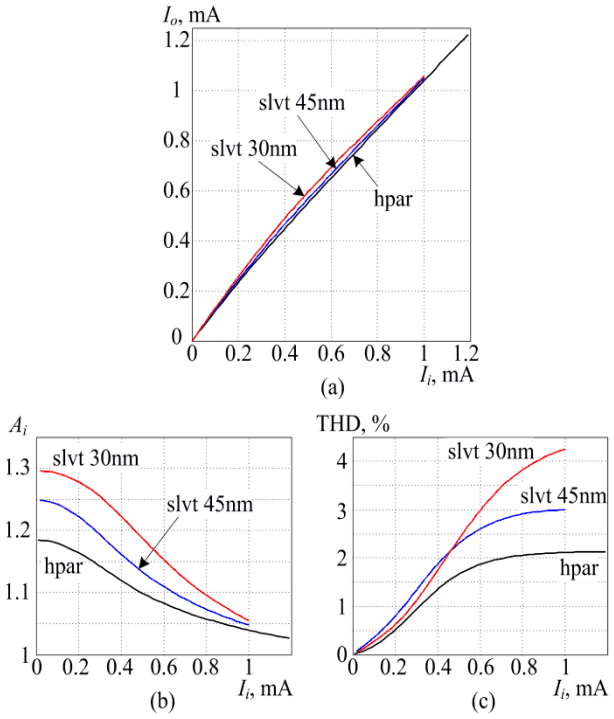


**Fig. 6 Dependences of large signal parameters of the designed amplifiers from the input current: (a) output current; (b) large signal current gain; (c) THD.**

The large signal behavior is illustrated in Fig. 6. They are obtained by parametric time domain analyses using sinusoidal input current source with parameterized amplitude. Its frequency is fixed at 10 KHz—low enough to avoid slew rate effects and suppression of the harmonics, generated in the amplifier, from its frequency response.

The dependence of the amplitude of the output current from the amplitude of the input current is shown in Fig. 6(a). The curves are very close to each other due to the approximately equal current gains of all three versions and it is difficult to distinguish them. For this reason two other characteristics are added: large signal current gain $A_i=I_o/I_i$ and the THD, both as functions of the input amplitude. These characteristics show that the decreasing of the channel length increases the nonlinearity. Evidently this is the price for the extended frequency bandwidth. However, the amplifier with hpar transistors has similar THD as the amplifier with three times longer (270 nm) zgfet transistors, which has 1.7% THD at $I_i = 1$ mA [6].

## 6. Conclusion

One of the most common current amplifiers is designed with three different types of deep submicron MOSFETs from a 32 nm CMOS technology: 90 nm hparfet, 45 nm and 30 nm slvtfet. The major benefit of short channel transistors is significant extension of the frequency bandwidth —up to 45 GHz for the circuit with shortest channel transistors. The large signal behavior is also investigated and the hpar version of the circuit shows similar non-linearity compared to the same circuit with much longer transistors. Certain increase of the non-linearity is observed for the versions with shorter channel transistors (slvtfets). The maximum amplitude of the input current is lower due to the reduced operating voltages of the used transistors, but this limitation can be relaxed by using wider FETs and higher biasing current.

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