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Feedback Filtering for Digital Control Applications

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Abstract: Thanks to the progress in semiconductor technologies, today microcontrollers offer huge computational power. That allows using advanced control algorithms with a built-in intelligence with a sufficient speed, for many demanding applications. These capabilities make the embedded control ideal for using at complex plants and for obtaining the highest performance in a wide area of operations. However, control performance also strongly depends on the feedback. A short latency and a high precision of embedded analog peripherals allow building fast and accurate control loops. The paper proposes an easy design method of high performance analog to digital converter filtering path, optimized for control applications.

Key words: ADC, digital control, anti-aliasing.

1. Introduction

To obtain a high performance regulation, plant state should be precisely and currently measured. Precision of measurement is limited by sensor conditioning and converting path, especially by ADC (analog to digital converter) and antialiasing filters. A phase delay produced by an analog low pas filter, together with times needed to: taking samples by ADC, filtering, conditioning, executing control algorithm calculations and establishing output, cause regulation delay and limit the regulation speed [1]. This paper shortly presents the author's experience in the area of designing high performance measurement path for digital control applications, explains meaning of aliasing for the control process and proposes a fast and easy designing method for designing antialiasing filters.

2. Feedback Interface Design

Most of effort during designing is used to optimal utilization of system capabilities. Optimal designing requires adequate understanding parts of the processing chain and its influence on the final results.

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2.1 Filtering Requirements

To achieve assumed precision, frequency characteristics of the measurement path should provide negligible aliasing effect of the sampling at the controller entrance.

Fig. 1 shows typical frequency characteristics requirements for the controller application. Sampling always results in aliasing of the signal components whose frequencies are higher than the half of the sampling frequency. For a proper conversion, the high frequency components should be dumped below output precision level. The aliasing doubles signal component at the Nyquist frequency, therefore, to avoid inaccuracy, the dumping factor at the half of regulation frequency must be greater about 6 dB:

$$D\left(\frac{f_R}{2}\right) = 20Log\left(\frac{1}{2^{ENOB_{OUT}+1}}\right) \quad (1)$$

where:

D-required filters dumping factor;

f_R -regulation frequency;

$ENOB_{OUT}$ -effective number of bits at output.

2.2 Analog Low Pass Filter

In control applications, non-oscillated Bessel filters are used, from 3rd to 7th order is usually applied with Sallen-Key or Multiple feedback topologies [2].

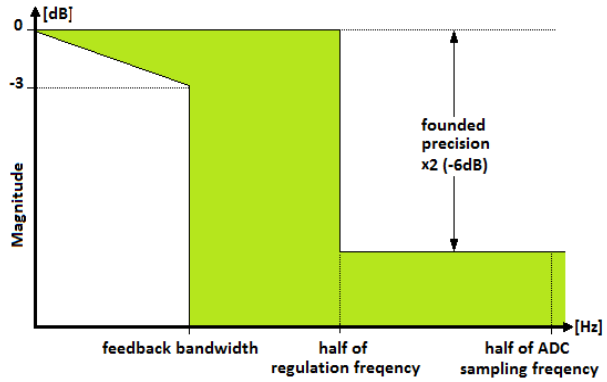

Fig. 1 Measurement path frequency requirements.

Table 1 presents dependence of required regulation frequency on the assumed accuracy (dumping level) and applied analog filter order. The low filter order results in a low phase delay and wide transition band. As can be seen lower filter order forces larger *N* with transfers to greater computing power consumption (control algorithm must to be executed more frequently).

2.3 Analog to Digital Converter

ADC is the key component of the whole interface chain. Sampling, conversion and digital data transfer times cause additional delay, strictly reducing regulation bandwidth. The ADCs *Effective Number of Bits* $ENOB_{ADC}$ limits feedback accuracy. Output resolution can be improved by oversampling and reducing output bandwidth in digital low pas filter. The accuracy achieved via oversampling is described by formula [3]:

$$NOB = 1.66 \cdot Log(OVSR) \qquad (2)$$

where:

OVSR-oversampling ratio;

NOB-number of archiving bits.

2.4. Digital filter and decimator

In order to achieve high accuracy control, the high dumping at the Nyquist frequency and above it is needed. Thanks to multi-bit precision, the digital FIR (finite impulse response) filters of high order can be realized providing a narrow transition band [4]. For control application, the minimum phase filter with aperiodic pulse response is desired.

If oversampling and filtering was used, the filtered signal should contain only regulation band components, so sampling frequency may be decreased to the controller execute frequency. In order to minimize computation time (by use simple algorithm), sampling frequency should be integral multiple of regulation frequency. In this case, the decimation process simplifies itself to calculate filter output ones at every control algorithm entrance.

3. Designing Example

Presented designing procedure was developed for achieving satisfactory results in simple process without laborious successive approximation method. Main procedure assumption is based on using digital FIR filter only with tap length corresponding to oversampling ratio. Under these conditions, flat Kaiser filter window will be executed as simple average of samples. Because the width of the filter window is equal to the regulation period, amplitude dumping at the half or regulation frequency is small (almost – 4 dB) and produced phase delay is close to 90 degrees.

Table 1 Filtering path results.

Accuracy	Require dumping level (dB)	Bessel filter order	
		3rd	5th
		Phase = 99.4°@ -3 dB	Phase = 140° @ -3 dB
5%	-26	*N*=8	*N*=6
2%	-40	*N*=13	*N*=8
1%	-46	*N*=17	*N*=10
0.5%	-52	*N* = 21	*N*=11

N-regulation frequency to measurement bandwidth ratio.

3.1 Embedded System Assumptions

Because every embedded system has some internal needs, e.g., tasks managements, only a part of computational power can be used for regulation purposes. This part can be named CPF (computing power factor). Also times requireded by the microcontroller core for execution every part of program can be specified:

T_{FIR}-FIR filter execution time per tab;

T_{LIN}-sensor linearization function time;

T_{REG}-regulation algorithm compute time.

Computing power utilization by control algorithms can be definite by equation:

$$CPF = f_R(N \cdot T_{FIR} + T_{LIN} + T_{REG}) \qquad (3)$$

where:

N-number of FIR tabs.

The ADC properties are specified by:

$ENOB_{ADC}$-effective number of bits (resolution);

$ADSR_{max}$-maximum samples rate per second.

Procedure will be executed for high speed and accurate temperature regulation example. For the purposes of example usual computing times of modern 100 MHz microcontroller are taken:

T_{FIR} = 0.1 µs; T_{LIN} = 1 µs; T_{REG} = 2 µs; CPF = 0.6;

Standard build in ADC will be used:

$ENOB_{ADC}$ = 9.4 bits; $ADSR_{max}$ = 1 Msps;

3.2 Maximum Speed with Embedded ADC Accuracy

Maximum regulation speed will be achieved without oversampling and digital filtering. Computing power utilization is expressed by Eq. (3) without filtering time contribution:

$$CPF = f_R(T_{LIN} + T_{REG})$$

Hence:

$$f_R = \frac{CPF}{T_{LIN} + T_{REG}} = \frac{0.6}{3\mu s} = 200kHz$$

Regulation precision is limited by $ENOB_{ADC}$ to the level of 0.15%. A required dumping of analog filter at half regulation frequency will be determined by using Eq. (1):

$$D(100\ \text{kHz}) = 20\ Log(\frac{1}{2^{ENOB_{ADC}}}) = -\ 62.6\ \text{dB}$$

Filtering is proceed with 3rd order Bessel filter of cut-off frequency fc = 6,600Hz (see Fig. 2).

3.3 Maximum Speed at Assumed Precision

Established precision of 0.01% corresponds to 13.3 bits of accuracy, therefore:

$$NOB = ENOB_{OUT} - ENOB_{ADC} = 13.3 - 9.4 = 3.9$$

Hence using Eq. (1):

$$OVSR = 10^{0.602 \cdot NOB} = 10^{0.602 \cdot 3.9} = 223$$

At high oversampling ratio regulation frequency is limited by ADC data rate:

$$f_R = \frac{ADSR_{MAX}}{OVSR} = \frac{1Msps}{223} \approx 4,484Hz$$

In this case computational power will not be fully used.

To achieve 0.01% of accuracy, filters magnitude should meet requirement of Eq. (1):

$$D(2{,}242\ \text{Hz}) = 20\ Log(\frac{1}{2^{13.3+1}}) = -\ 86.1\ \text{dB}$$

Kaiser digital filter of 222nd order will produce -4 dB of dumping at half of regulation frequency, hence analog filter is responsible for providing the rest of required dumping level (– 82.1 dB). This will be done with 7th order Bessel filter of cut-off frequency f_C = 320 Hz (see Fig. 3).

3.4 Optimal System Capabilities Usage

Regulation frequency could be optimized to achieving higher sensor signal resolution, by using maximum ADC data rate:

$$f_R \cdot OVSR = ADSR_{MAX} \qquad (4)$$

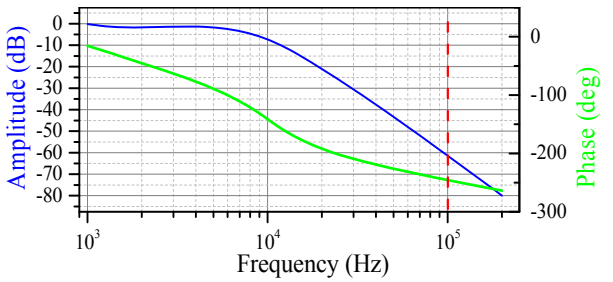

Fig. 2 Maximum speed design results.

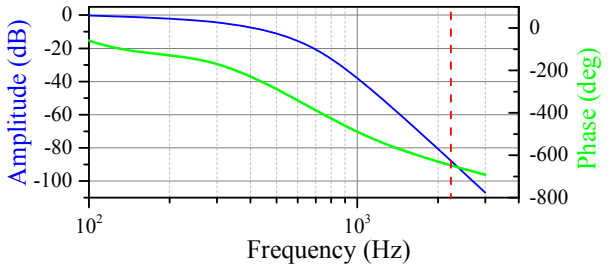

Fig. 3 High oversamplin design results.

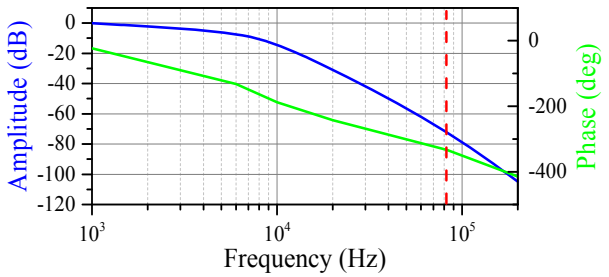

Fig. 4 Optimum system usage results.

Computing power Eq. (3) with FIR length equals the oversampling ratio is given by:

$$CPF = f_R(OVSR \cdot T_{FIR} + T_{LIN} + T_{REG}) \quad (5)$$

Using Eqs. (4) and (5), we have:

$$f_R = \frac{CPF - ADSR_{MAX} \cdot T_{FIR}}{T_{LIN} + T_{REG}} = \frac{0.5}{3\mu s} = 166kHz$$

$$OVSR = \frac{ADSR_{MAX}}{f_R} = \frac{1Msps}{166kHz} = 6$$

Signal precision is defined by Eq. (2):

$$ANOB_{OUT} = ANOB_{ADC} + 1.66Log(OVSR) =$$
$$= 9.4 + 1.66Log(6) = 10.7[bits]$$

resulting in 0.06% of output accuracy. The required of filters dumping is specified by the equation [1]:

$$D(83kHz) = 20Log\left(\frac{1}{2^{10.7+1}}\right) = -70.4dB$$

Kaiser digital filter of 5th order will produce -3.8 dB of dumping at half of regulation frequency, so analog filter need to provide remaining -66.6 dB of dumping. It will be done with 3rd order Bessel filter of cut-off frequency *fc* = 4,600 Hz. (see Fig. 4).

4. Conclusion

The paper explains feedback filtering necessity and shows designing approaches to satisfy different regulation needs. Presented easy-design-method provides good results especially for fast regulation with moderate oversampling.

References

[1] Phillips, C. L., Nagle, T., and Chakrabortty, A. 2014. *Digital Control Analysis and Design.* New Jersey: Prentice Hall.

[2] Williams, A. 2013. *Analog Filter and Circuits Design Handbook.* United States: McGraw-Hill Professional.

[3] Lyons, R. G. 2010. *Understanding Digital Signal Processing.* New Jersey: Prentice Hall.

[4] Smith, S. 2002. *Digital Signal Processing-A Practical Guide for Engineers and Scientist*. Boston: Newnes